Lecture 1

Diodes

- two-terminal device: one current, one voltage

  $P = IV$ → if $P > 0$: absorbing / dissipating pwr
  $P < 0$: supplying pwr

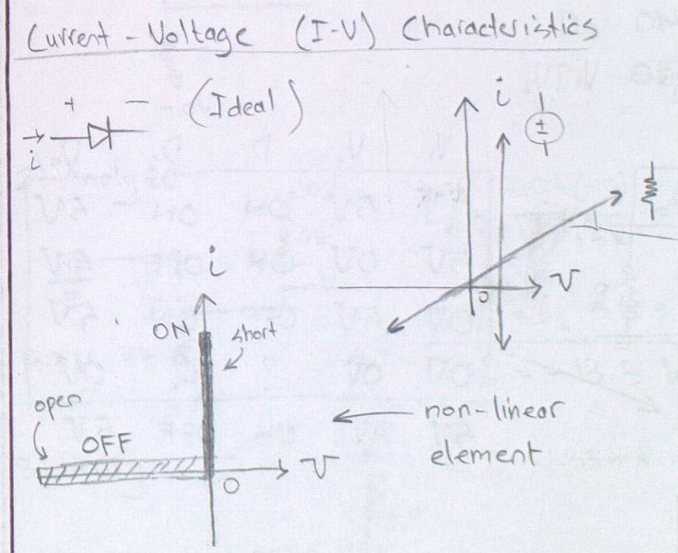
- diode: a valve, lets current flow only in one direction (from anode to cathode)

- ideal diode : → short ckt when ON (conducting)
  → open ckt when OFF (not conducting)

Lecture 2

Sep 4, 2024

Current - Voltage (I-V) Characteristics



Voltage src:

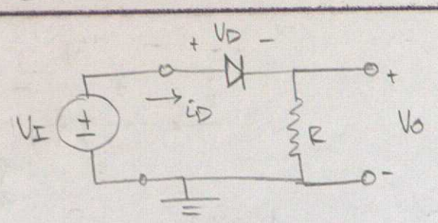
current src:

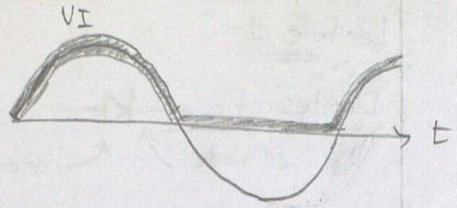
slope: $\frac{1}{R} = G$ (conductance)

Ideal Diode

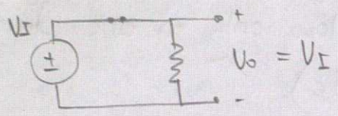
on

OFF



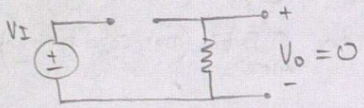


- when V_I high, i flows (voltage at anode high)
- when V_I low, i stops flow (voltage at anode low)

ON: 

"output same as input"

$V_I > 0$ = 'ON'

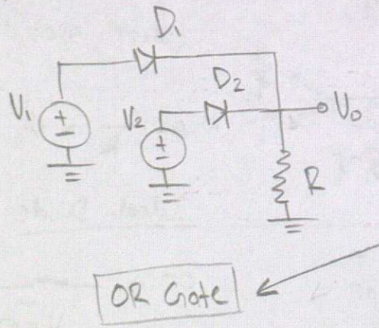
OFF: 

"output is zero"

$V_I < 0$ = 'OFF'

- half-wave rectifier with one diode

→ Eg 1: Find V_o given V_1, V_2

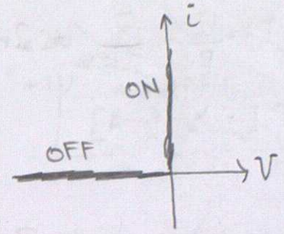


OR Gate

V_1	V_2	D_1	D_2	V_o
5V	5V	ON	ON	5V
5V	0V	ON	OFF	5V
0V	5V	OFF	ON	5V
0V	0V	?	?	0V
5V	4V	ON	OFF	5V

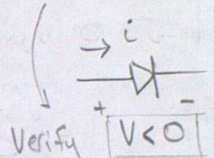
- Assume an operating region → Analyze → Verify

Analysis Process



OFF

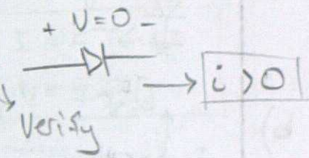
Assume $i = 0$



Verify $V < 0$

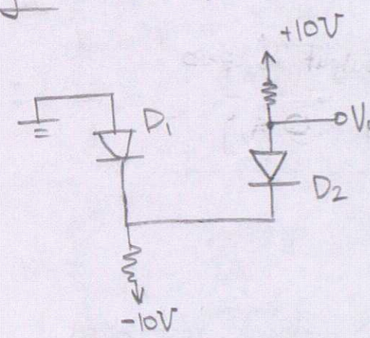
ON

Assume $V = 0$



Verify

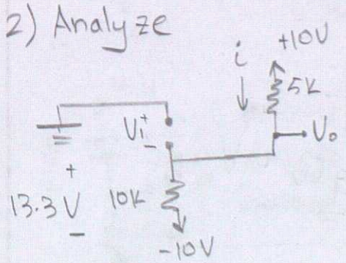
② Eg: Find V_o



- We can discard possibility of both diodes being OFF since D_2 will be ON.

1) Assume
D_2 ON
D_1 OFF

2) Analyze

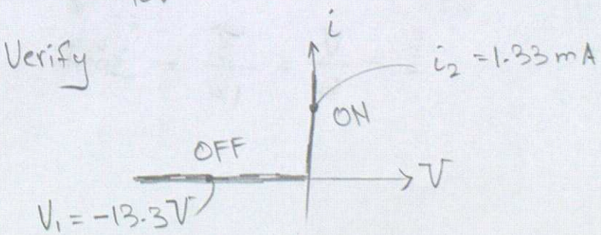


$$i_2 = \frac{+10-(-10)}{10K+5K} = 1.33\,mA$$

$$\therefore V_o = i_2 \cdot 5K = 3.3\,V$$

$$V_1 = -13.3\,V$$

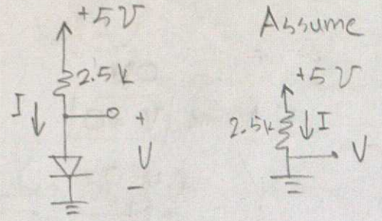
3) Verify



Assumption of D_1 OFF and D_2 ON is correct

Exercises (4, 5)

✓ 4.4.a)

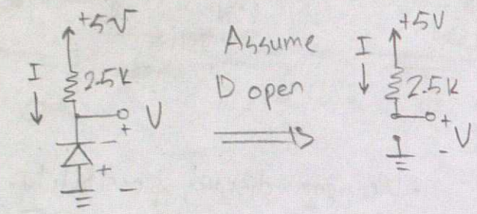


Assume D closed

$V = IR \Rightarrow I = \frac{V}{R} = \frac{5}{2.5k} = 2mA$

$V = 0$ [V] $I = 2$ [mA]

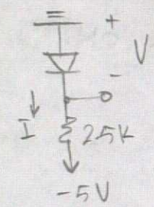
b)



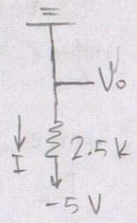
Assume D open ⟹

$I = 0$
$V = 5$ [V]

d)



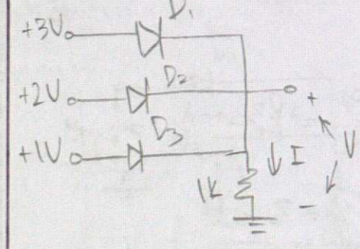
Assume D on ⟹



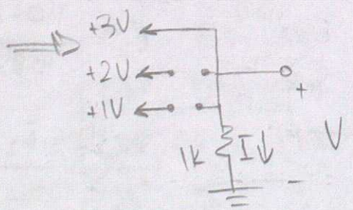
$I = 2$ [mA]
$V = 0$ [V]

e)

Q: in general, do we close larger V node?



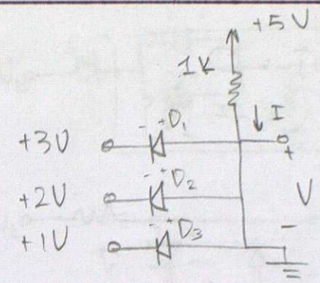
Assume D_1 closed, rest open ⟹



$V = 3$ [V]
$I = 3$ [mA]

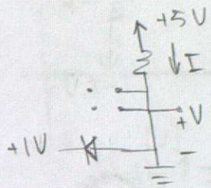
$I = \frac{V}{R} = \frac{3}{1k} = 3mA$

f)



$I = \frac{V}{R} = \frac{5-1}{1k} = 4$ [mA]

Assume D_1, D_2 open and D_3 closed



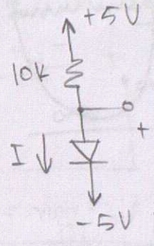
$5 - 1 = 4V$

$I = 5$ [mA]
$V = 1$ [V]

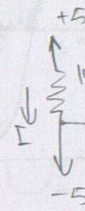
Problems (2, 4, 7, 9)

4.2.a)

▷



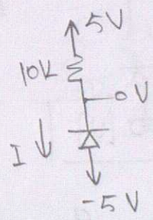
Assume closed ⟹



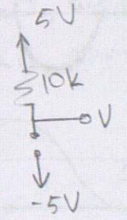
$I = \frac{5-(-5)}{10k} = 1$ mA

$V = -5$ [V]
$I = 1$ [mA]

✓ b)

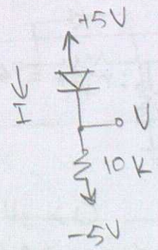


Assume Open ⟹

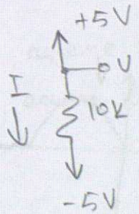


$I = 0$
$V = 5V$

✓ c)

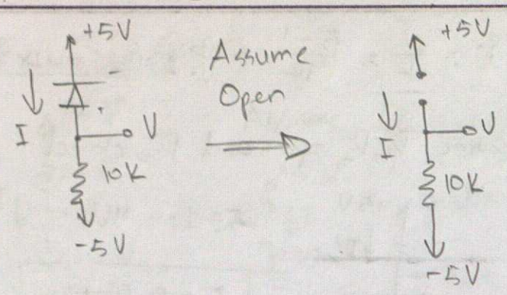


Assume Closed ⟹

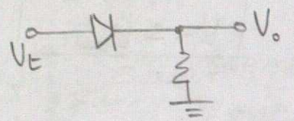


$I = \frac{5-(-5)}{10k} = 1$ mA

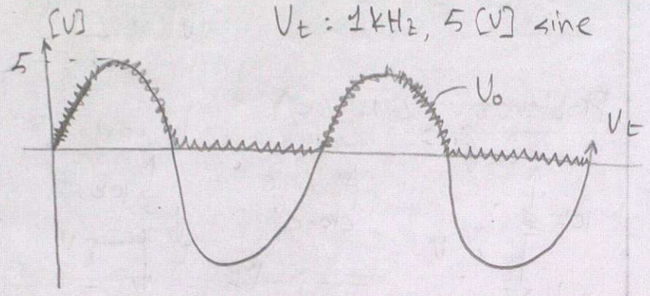
$I = 1$ [mA]
$V = 5$ [V]

d) 

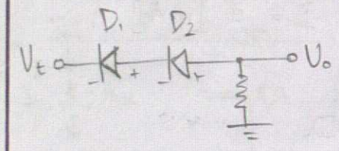
$I = 0$
$V = -5$ [V]

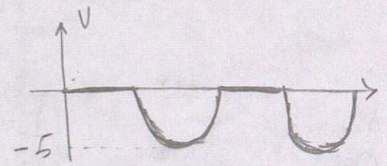
4.4.a) 

Q: Can I draw V_o on top of V_t?

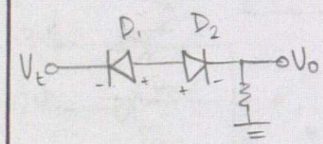


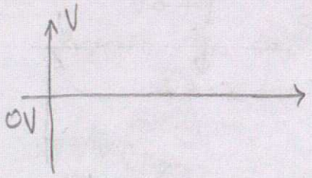
V_o : max = 5 [V]

b) 

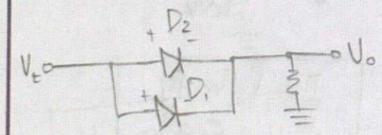


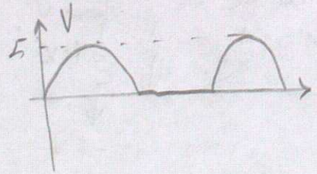
V_o : min = -5 [V]

c) 

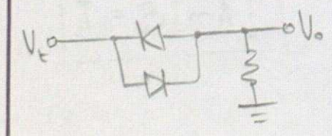


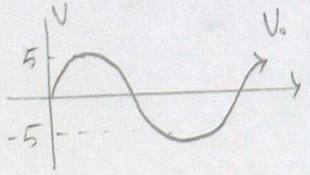
V_o : 0 [V]

d) 

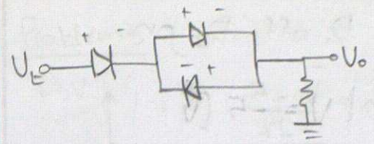


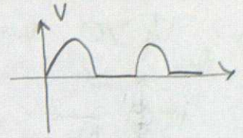
V_o : max = 5 [V]

e) 

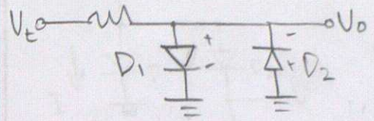


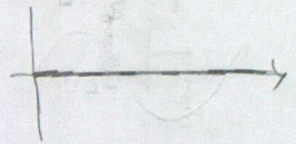
V_o : max = 5 [V]
min = -5 [V]

f) 

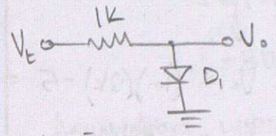


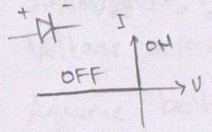
V_o : max = 5 [V]

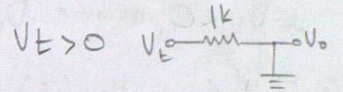
h) 



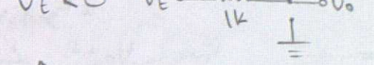
V_o : max = 0 [V]
min = 0 [V]

g) 

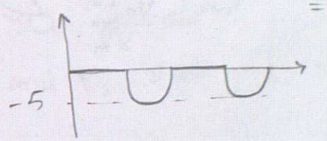


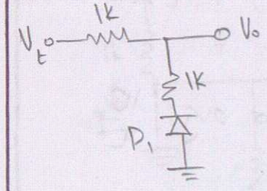
$V_t > 0$ 

$V_o = 0$ [V]

$V_t < 0$ 

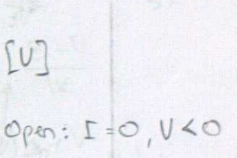
Assume Open: $I = 0, V < 0$

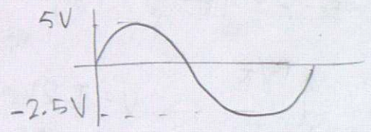


i) 

$V_t > 0$, assume off: $I = 0, V_o > 0$

$V_t < 0$, assume on: I , $V < 0$

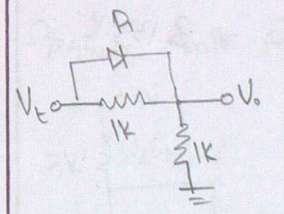




$\frac{-5 - V_o}{1k} + \frac{0 - V_o}{1k} = 0$

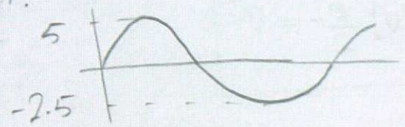
$\frac{-5 - V_o}{1k} = \frac{V_o}{1k}$

$V_o = -2.5$

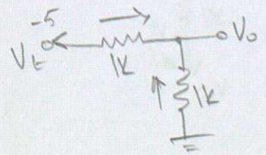
j) 

$V_t > 0$, assume on: $I > 0, V_o = V_t$

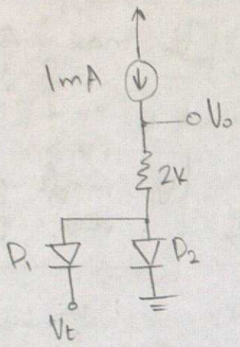
$V_t < 0$, assume off:



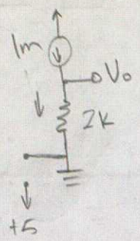
$V_t < 0$



k)

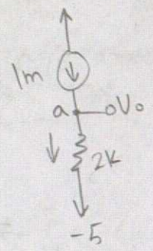


$V_t > 0$, assume D_1 off, D_2 on



$$I_m = \frac{V_o - 5}{2k}$$

$V_t < 0$, assume D_1 on, D_2 off



KCL @ 2: $I_m = \frac{V_o - (-5)}{2k}$

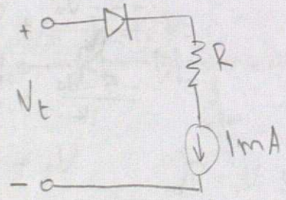
$$I_m = \frac{V_o + 5}{2k}$$

$$V_o = (I_m)(2k) - 5 = -3$$

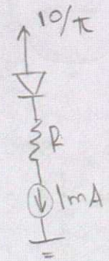
$$V_o = -3V$$

Excersizes (5)

4.5



V_t: 20V peak-to-peak, so avg: $\frac{10}{\pi}$

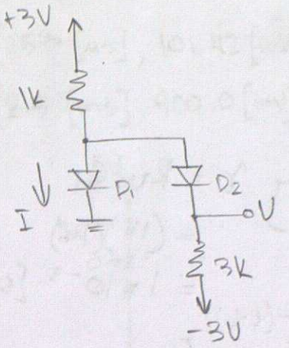


$$V = IR$$

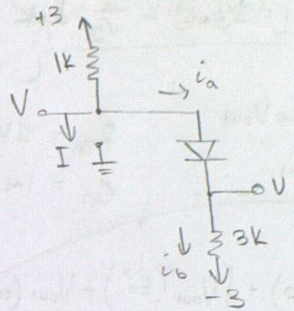
$$R = \frac{10/\pi}{I_m} = 3.133\,K\Omega$$

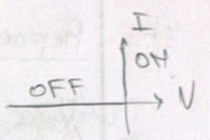
Problems (7.9)

4.7.a)



Assume D_1 off and D_2 on





$$i_a = \frac{3 - V}{1K}$$

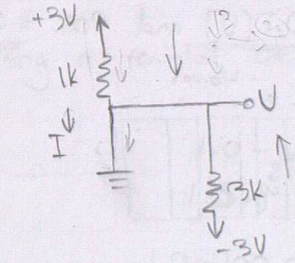
$$i_b = \frac{V - (-3)}{3K} = \frac{V+3}{3K}$$

$$\frac{V+3}{3K} = \frac{3-V}{1K}$$

$$\frac{1}{3}V + 1 = 3 - V$$

$$\frac{4}{3}V = 2 \Rightarrow V = \frac{3}{2}$$

Assumption wrong since Voltage across $D_1 > 0$, so now Assume both D_1 and D_2 ON

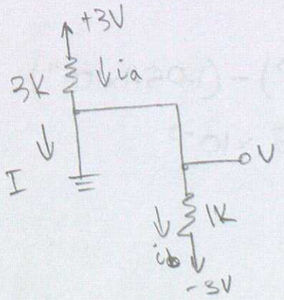


All the current goes straight to ground since the D_1 path has the least resistance

$$I = \frac{3}{1k} = 3\,mA$$

$$\therefore I = 3\,[mA]$$
$$V = 0\,[V]$$

b) Assume both ON



$$i_a = \frac{3-V}{3K} \qquad i_b = \frac{V+3}{1K}$$

$$\frac{3-V}{3k} = \frac{V+3}{1K}$$

$$1 - \frac{1}{3}V = V + 3$$

$$-2 = \frac{4}{3}V$$

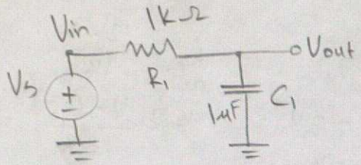
$$-\frac{3}{2} = V$$

$$I = 0\,[A]$$
$$V = -\frac{3}{2}\,[V]$$

Preparation Exercise

$V_{RMS} = \frac{1}{\sqrt{2}} V_{pk}$ $\quad I_{RMS} = \frac{1}{\sqrt{2}} I_{pk}$

PE1.)



$R_{Th} = 1k$, $C_1 = 1\mu$ $\Rightarrow \tau = R_{Th} C_1 = (1k)(1\mu) = 1 \times 10^{-3}$ [s]

$V_{out}(t) = V_{out}(\infty) + \left[V_{out}(t_0^+) - V_{out}(\infty)\right] e^{-(t-t_0)/\tau}$

$V_{out}(\infty) = 1$ [V], $V_{out}(t_0^+) = 0$ [V]

$\therefore V_{out}(t) = 1 - e^{-t/0.001}$

Since final value is 1 [V], 10% is 0.1 [V] and 90% = 0.9 [V]

$0.1 = 1 - e^{-t/0.001}$

$e^{-t/0.001} = 0.9$

$-\frac{t}{0.001} = \ln 0.9$

$t = -0.001 \ln 0.9$

$t_{0.1} = 1.054 \times 10^{-4}$ [s]

$0.9 = 1 - e^{-t/0.001}$

$-e^{-t/0.001} = -0.1$

$-\frac{t}{0.001} = \ln 0.1$

$t = -0.001 \ln 0.1$

$t_{0.9} = 2.3 \times 10^{-3}$ [s]

Rise time is $t_{0.9} - t_{0.1} \Rightarrow (2.3 \times 10^{-3}) - (1.054 \times 10^{-4})$

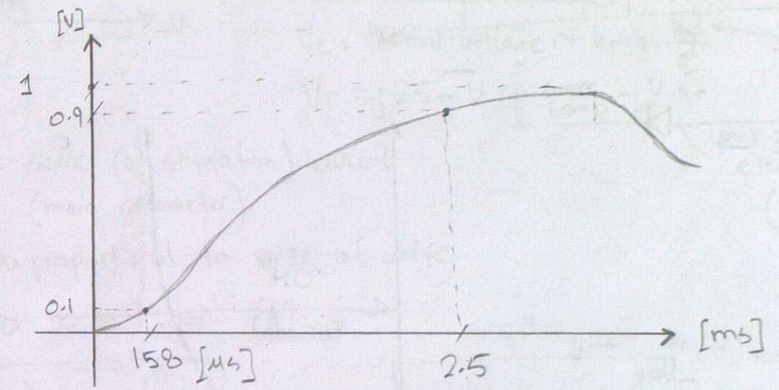
$= 2.195 \times 10^{-3}$

$\therefore \tau = 0.001$ [s]

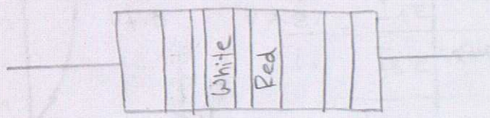
$t_r = 2.195$ [ms]

PE2.1) V_s : 100 Hz, 0V–1V pulse, 0.1 ms rise & fall times

2.2) (158 [μs], 101.42 [mV]), (2.5 [ms], 900.0 [mV]) $\Rightarrow$ $t_r = 2.5$ [ms] $\quad \Delta V = 798$ [mV]

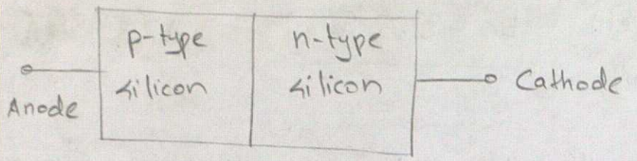


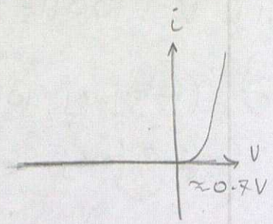
2.3 Using a resistor of 900 Ω, we get $t_r = 2.09$ [ms]

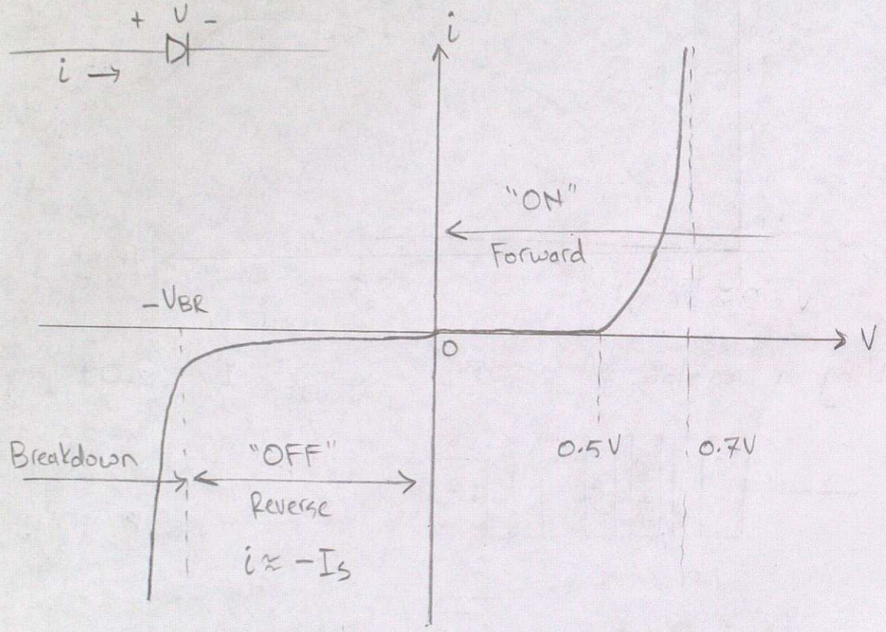


Ch. 4.2

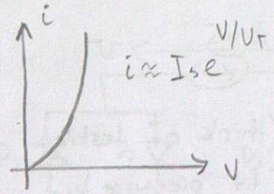
PN Junction Diode







Forward bias region (V>0)



$$i = I_S\left(e^{\frac{V}{V_T}} - 1\right)$$

V_T : thermal voltage $V_T = \frac{kT}{q}$

$V_T \approx 25\,mV$ @ room temp

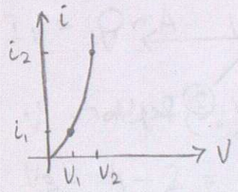
k: Boltzman Constant $(1.38\times10^{-23}\ \frac{J}{K})$

T: temp of junction (300K / 27°C)

q: unit electron charge $(1.602\times10^{-19}\,C)$

I_S: scale (or saturation) current (main parameter)
- ↳ proportional to size of wire
- ↳ $\approx 10^{-9} - 10^{-15}$ [A]

$$i \approx I_S e^{V/V_T} \Longrightarrow V = V_T \ln\left(i/I_S\right)$$



$$\frac{i_2}{i_1} = \frac{I_S e^{V_2/V_T}}{I_S e^{V_1/V_T}} = e^{\frac{V_2 - V_1}{V_T}}$$

or $V_2 - V_1 = V_T \ln\left(i_2/i_1\right)$

go to base 10, add a ln(10) scale factor

$$V_2 - V_1 = V_T \ln(10) \log_{10}\left(i_2/i_1\right)$$

$\approx 25mV$ × ≈ 2.303 $\approx 60\,mV$

i	V	
1 mA	0.7V	+60mV
10mA	0.76 V	+60mV
100mA	0.82 V	
↓ go small		
0.1mA	0.64 V	

(×10 ↳ ×10 ↳)

- even if i increase a lot, ΔV isn't much

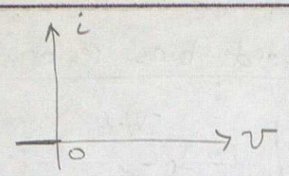
temperature

for the same current:

−2mV / 1°C temp increase

Reverse bias region ($V<0$)

$$i = I_S\left(e^{V/V_T} - 1\right)$$

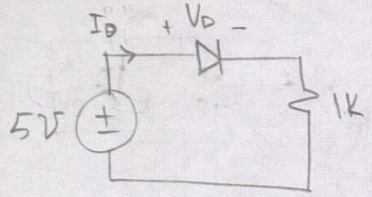


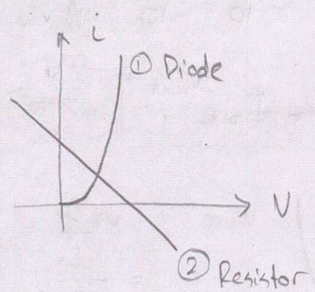
$i \approx -I_S$ ← small but not zero (think of leaking in opp. direction due to pressure)

- might say "not I_S, but $I_S \to I_{REVERSE}$ (still small)

I

Eg: Calculate V and i of pn-junction. $V = 0.7V$ @ $1\,mA$ and $V_T = 25\,mV$





Assume forward bias

$$I_D = I_S e^{V_D/V_T} \quad (1)$$

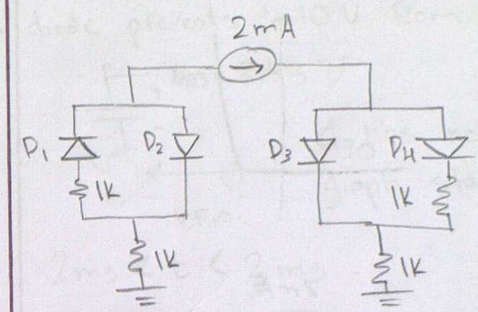
KVL: $5 = V_D + I_D \cdot 1k$

$$-5 + V_D + I_D \cdot 1k = 0$$

$$I_D = -V_D + 5 \quad (2)$$

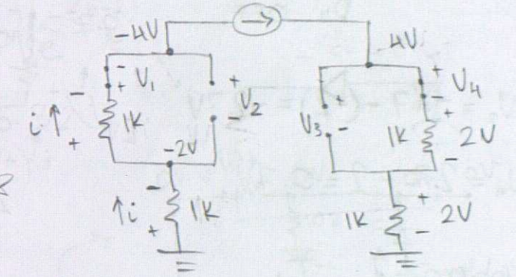
Tutorial 1 — Sep 11, 2024

Problem 1



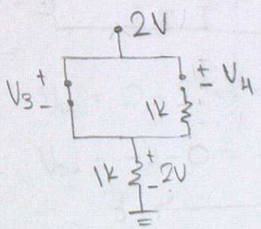
a) Assume diodes ideal

$I_1 = 2\,mA$	$V_1 = 0\,V$	
$I_2 = 0\,mA$	$V_2 = -2V$	
$I_3 = 2\,mA$	$V_3 = 2V$	★
$I_4 = 0\,mA$	$V_4 = 0\,V$	



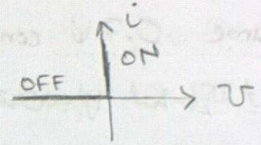
$V_2 = -4 - (-2) = -2\,V$

$V_3 = 4 - 2 = 2V$ ← D_3 "off", so should have been <0



$V_4 = 2 - 2 = 0$

a)



Assume:		check
D_1	ON	✓
D_2	OFF	✓
D_3	OFF	× ON ✓
D_4	ON	× OFF ✓

Sep 11 2024

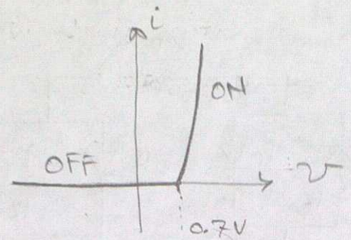
b) Assume 0.7 V constant drop across diode

$I_1 = 2mA \quad V_1 = 0.7V$

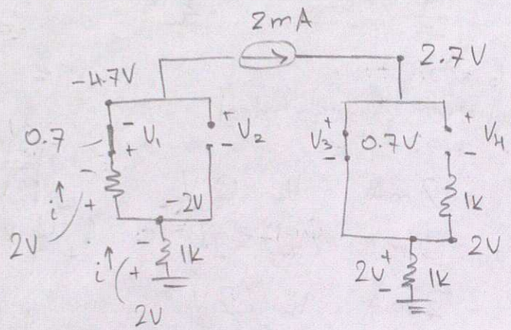
$I_2 = 0mA \quad V_2 = -2.7V$

$I_3 = 2mA \quad V_3 = 0.7V$

$I_4 = 0mA \quad V_4 = 0.7V$



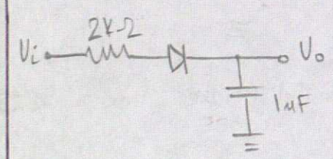
Assume D_1 ON
D_2 OFF ✓
D_3 ON
D_4 OFF

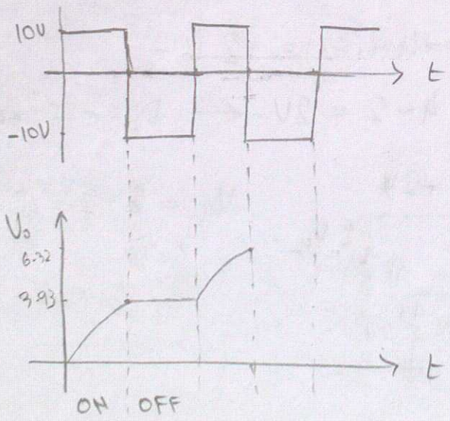


$V_2 = -4.7 - (-2) = -2.7V$ ✓

$V_4 = 2.7 - 2 = 0.7V$ ✓

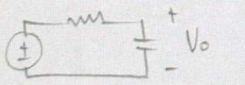
Problem 2





$\tau = (2k)(1\mu) = 2\ ms$

$0 \le t < 1ms$



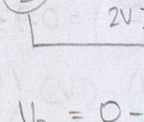
$V_o = \cancel{V_o(\infty)}^{10V} + \left(\cancel{V_o(t_0^+)}^{0V} - \cancel{V(\infty)}^{10V}\right) e^{-t/\tau}$

$V_o = 10\left(1 - e^{-t/2m}\right)\ [V]$

$V_o(1ms) = 3.93\ V$

$1ms < t < 2ms$

- diode prevents −10 V from pulling current to left



C has nowhere to discharge, so V_o graph stays flat.

$2ms < t < 3ms$

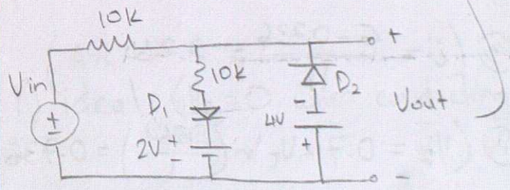
$V_o = V_o(\infty) + \left[V_o(t_0^+) - V(\infty)\right] e^{-\frac{(t-t_0)}{\tau}}$

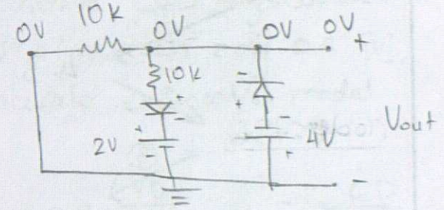
$V_o = 10 + \left[10(1-e^{-1/2}) - 10\right] e^{-\frac{(t-2)}{\tau}}$

$V_o(3ms) = 10(1-e^{-1}) = 6.32\ V$

Question 2

a) $V_{IN} = 0V$





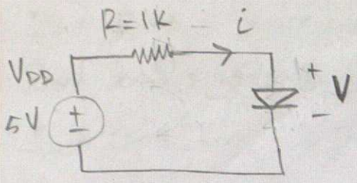
Assume D_1 OFF
D_2 OFF

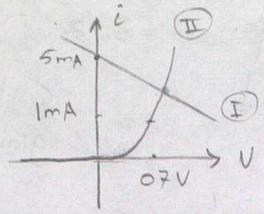
$V_{D1} = 0 - 2 = -2V < 0$, so D_1 OFF

$V_{D2} = -4 - 0 = -4V < 0$, so D_2 OFF

$\therefore V_{out} = 0V$

I **Eg:** Calculate I_D and V_D and diode voltage is 0.7 V at 1mA and $V_T = 25\,mV$.





circuit equation: $i = \frac{V_{DD} - V}{R}$ ①

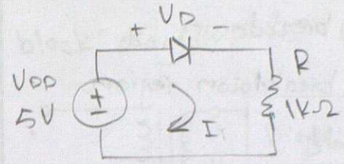
diode equation: $V_2 - V_1 = V_T \ln\left(\frac{i_2}{i_1}\right)$ ⑪

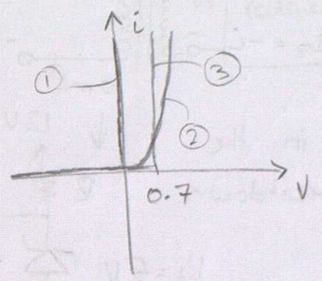
Unit sets [V, mA, K-Ω]

V [V]		i [mA]	
0.7	①	1	① $\left(i = \frac{5-0.7}{1K} = 4.3\ mA\right)$
		4.3	
0.736	②		② $\left(V_2 = 0.7 + V_T \ln\left(\frac{4.3}{1}\right) = 0.736\ V\right)$
	③	4.264	③ $\left(i = \frac{5-0.736}{1K} = 4.264\ mA\right)$
0.736	④		⑪ $\left(V_2 = 0.7 + V_T \ln\left(\frac{4.264}{1}\right) = 0.736\ V\right)$

solution: $i = 4.264\,[mA]$ and $V = 0.736\,[V]$

4.3 Forward Bias Diode Models



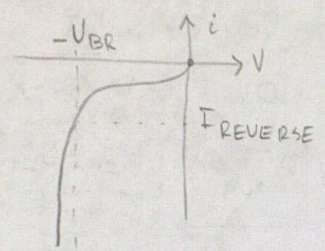


	Model	V_D	I
①	Ideal	0V	5 mA
②	Exponential (exact)	0.738 V	4.262 mA
③	Constant Voltage Drop (CVD)	0.7V	4.3 mA

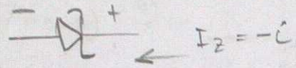
- CVD is similar to a shifted ideal voltage model.
- Say you have 2 diodes and 1 [V] source. CVD says diodes won't be on since voltage divides gives each only 0.5 [V], so you'll have to use the more accurate exponential model

	V_D	i_D
1) ideal ($V_D = 0$ when conducting)	0V	$\frac{5-0}{1K} = 5\,mA$
2) CVD ($V_D = 0.7$ V when conducting)	0.7V	$\frac{5-0.7}{1K} = 4.3\,mA$
3) exponential ($i_D = I_S e^{V_D/V_T}$)	0.736 V	4.264 mA

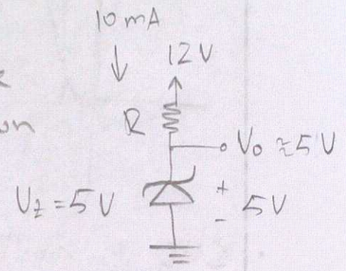
Breakdown Region



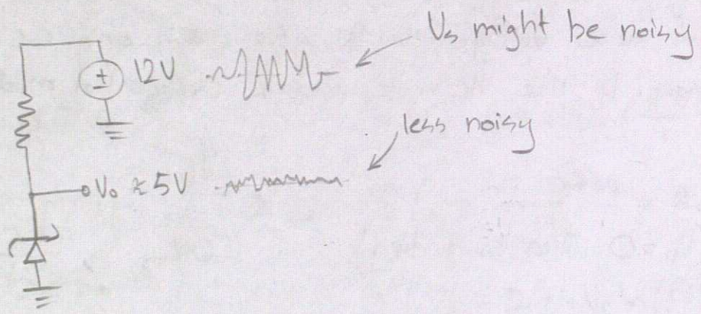
- avalanch breakdown
- diode in breakdown region
- Zener diode



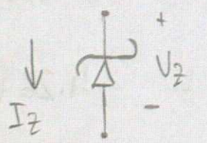
- Zener diodes are designed to operate in the breakdown region and ∴ have lower breakdown voltage, now called "Zener voltage" V_z



$$R = \frac{12 - 5\ V}{10\ mA} = 700\ \Omega$$

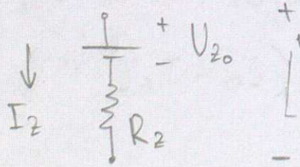


Zener diode symbol



diode is reverse biased

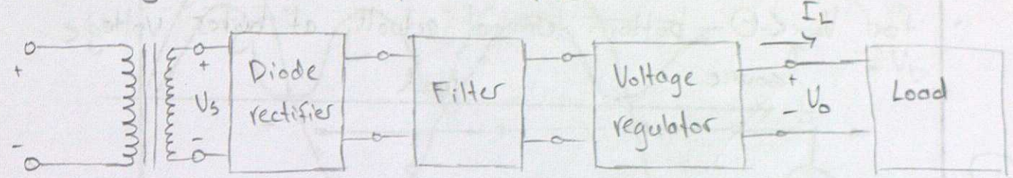
model for Zener diode



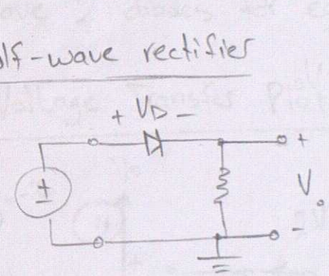
$$V_z = V_{z0} + R_z I_z$$

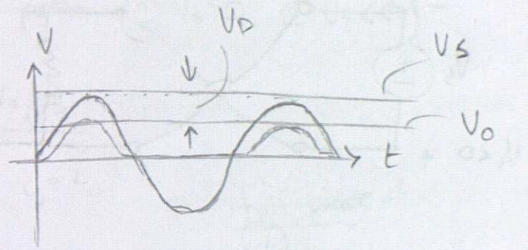
4.6 Rectifier Circuits

- block diagram of DC power supply

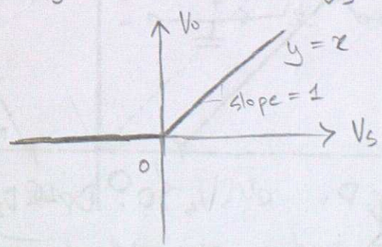


- half-wave rectifier



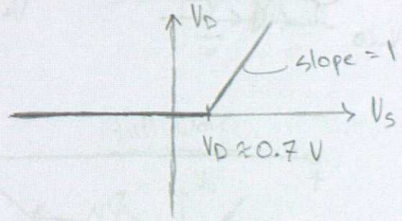


Voltage transfer plot, $\frac{V_O}{V_S}$



Ideal Diode

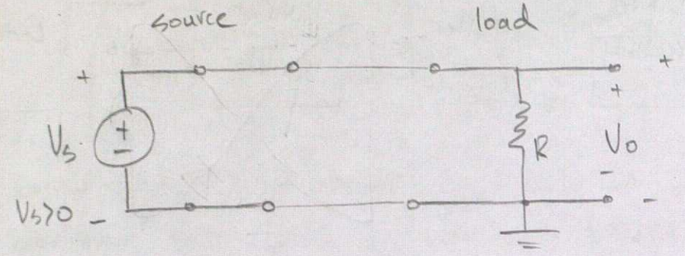
(including 0.7 V offset)



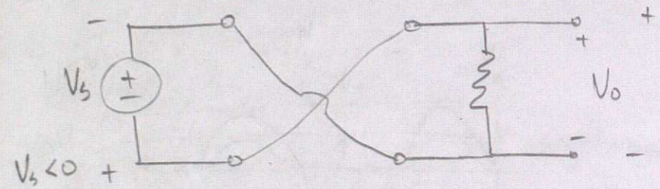
Actual Diode

Full-wave rectifier

- half-wave rectifier worked fine if $V_s > 0$, but what of $V_s < 0$?
- for $V_s < 0$, bottom terminal actually at higher voltage

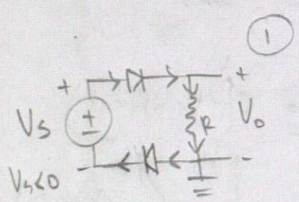


(I)

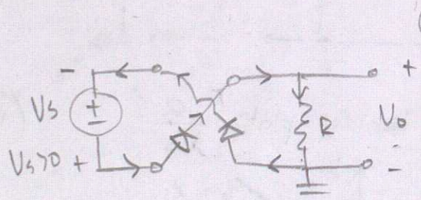


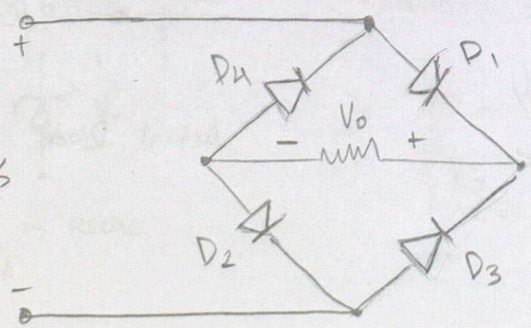
(II)

(I)



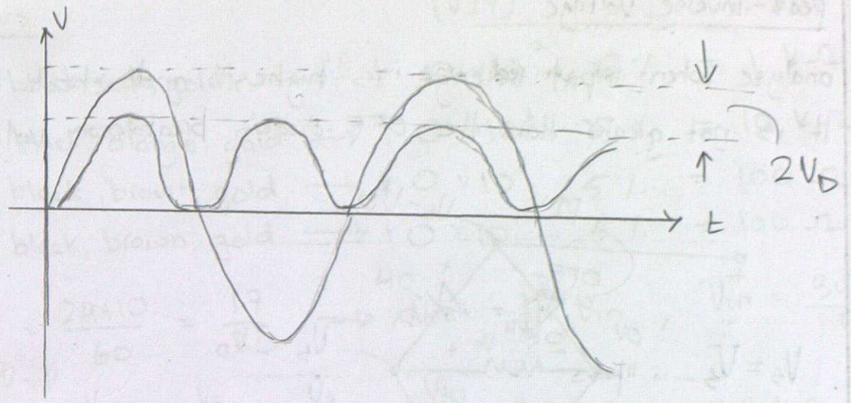
(II)





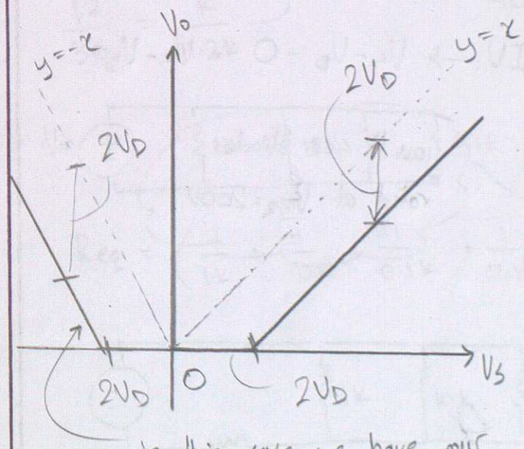
$V_s > 0$: $D_1 \rightarrow D_2$

$V_s < 0$: $D_3 \rightarrow D_4$



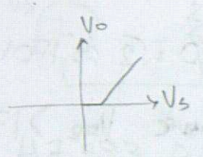
- Full-wave rectifier has $2V_D$ voltage drop since we have 2 diodes for each path (I $V_s > 0$, II $V_s < 0$)

Voltage Transfer Plot, V_o/V_s

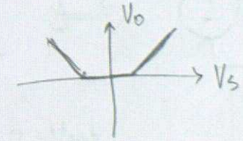


in this case, we have our plot mirrored on the negative side of V_s since V_o can extract a negative V_s into a positive voltage

half-wave

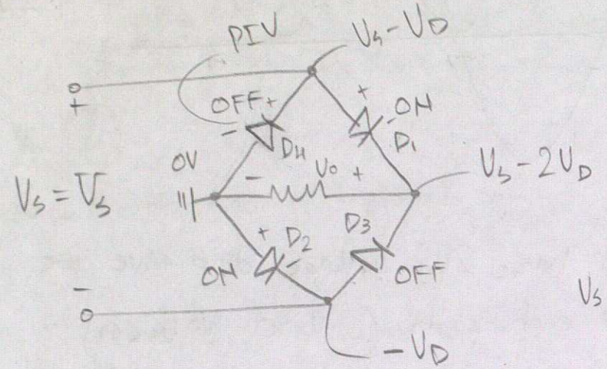


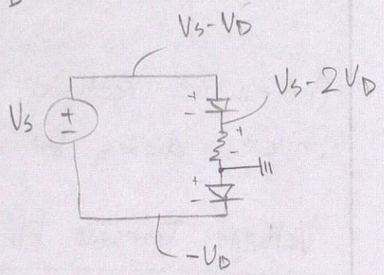
full-wave



peak-inverse voltage (PIV)

- analyze when input voltage is highest and check that it is not greater than the OFF-diode's breakdown voltage.





Now we can check V_{D4}

↳ peak inverse voltage: PIV → $V_s - V_D - 0 = V_s - V_D$

- for $120 \times \sqrt{2} \approx 170V$

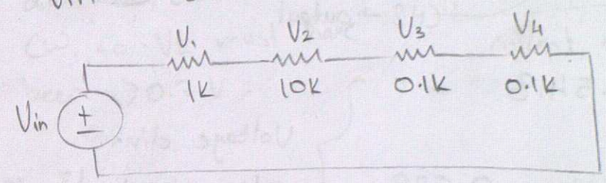
∴ Ensure $V_{BR} > 170V$

you'll see diodes rated at $V_{BR} = 200V$

E1.2 Resistors

1. brown, black, red, gold → 10×10^2 5% = 1 kΩ
2. brown, black, orange, gold → 10×10^3 5% = 10 kΩ
3. brown, black, brown, gold → 10×10^1 5% = 100 Ω = 0.1 kΩ
4. brown, black, brown, gold → 10×10^1 5% = 100 Ω = 0.1 kΩ

E1.3 $\frac{V_{out}}{V_{in}} = \frac{24+10}{60} = \frac{17}{30} \Rightarrow V_{out} = \frac{17}{30} V_{in}$, $V_{in} = \frac{30}{17} V_{out}$



$R_{eq} = 11.2\,k\Omega$

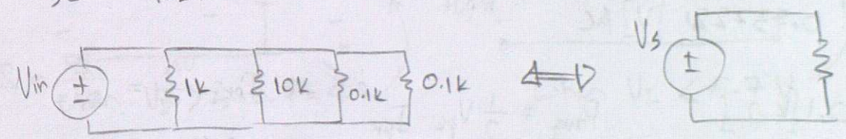
$V_{out} = \frac{R}{11.2k\Omega} \cdot V_{in}$

$V_{out} = V_{out}$

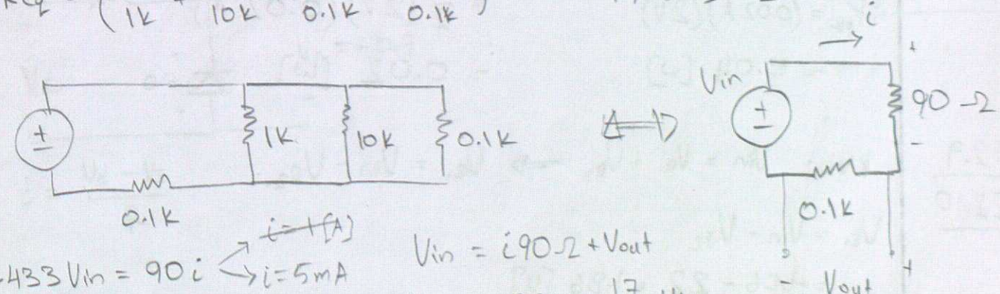
$\frac{17}{30} = \frac{R}{11.2k}$ → $R = \frac{17(11.2k\Omega)}{30} = 6346\,\Omega$

$(V_{out})_{ep} = 0.5827V$

$(V_{out})_{ic} = 0.529\,V$



$R_{eq} = \left(\frac{1}{1k} + \frac{1}{10k} + \frac{1}{0.1k} + \frac{1}{0.1k}\right)^{-1} = 47.393\,\Omega$



$0.433 V_{in} = 90i$ → ~~$i = 1$ [A]~~ → $i = 5mA$

$V_{in} = \frac{90}{0.433} = 1.039$

$V_{in} = 1.039\,V$

$V_{in} = i90\Omega + V_{out}$

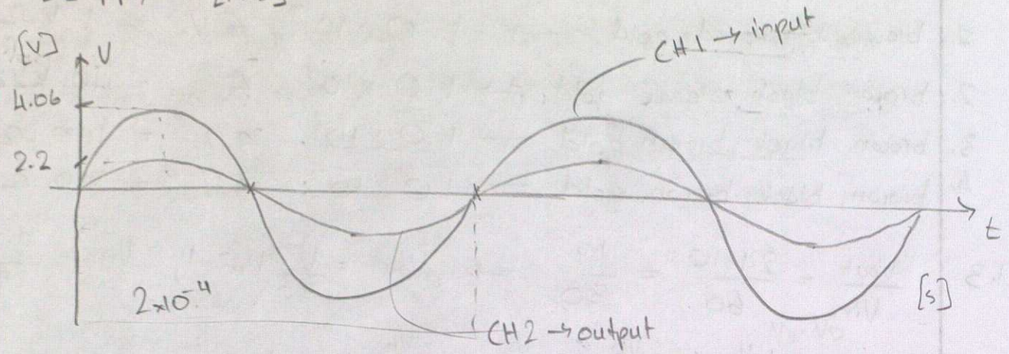
$V_{in} = i90\Omega + \frac{17}{30} V_{in}$

$V_{in} - \frac{17}{30} V_{in} = 90\Omega i$

$V_{in}\left(1 - \frac{17}{30}\right) = 90\Omega i$

E2.1 4 [V] PP, 5 [kHz]

E2.6



$\frac{V_{out}}{V_{in}} = \frac{2.2}{4.06} = 0.5418$

from E1, measured ratio = 0.529

} Voltage division ratio original: $\frac{17}{30} = 0.566$

E2.7 input: 1.4088 [V] AC

output: 0.73722 [V] AC

$\frac{\text{output}}{\text{input}} = 0.5233$

E2.8 $R_2 = 0.1\,[k\Omega]$

$P_{PK} = (0.02\,A)(2\,V)$

$= 0.04\,[W]$

$P_{avg} = \frac{1}{2} V_{PK} \cdot I_{PK}$

$= \frac{1}{2}(2\,V)(0.02\,A)$

$= 0.02\,[W]$

$I_{PK} = \frac{V_{PK}}{R} = \frac{2}{0.1k} = 2\,mA$

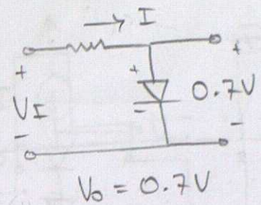
E2.9 / E2.10 KVL: $V_{in} = V_{R_1} + V_{R_2} \Rightarrow V_{R_1} = V_{in} - V_{R_2}$

$V_{R_1} = V_{in} - V_{R_2}$

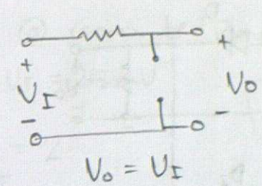
$= 4.06 - 2.2 = 1.86\,[V]$

Tutorial 2

Problem 1

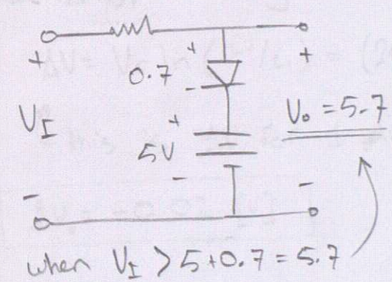
1) 

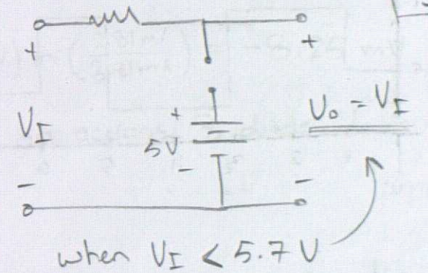
this happens when diode on, current flows CW, so V_I must have been > 0.7 V

or 

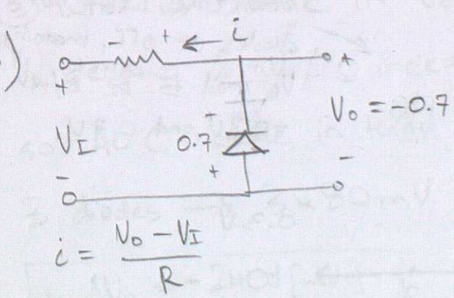
if V_I is less than 0.7V, diode off, no current, so $V_o = V_I$

∴ graph b

2) 



∴ graph d

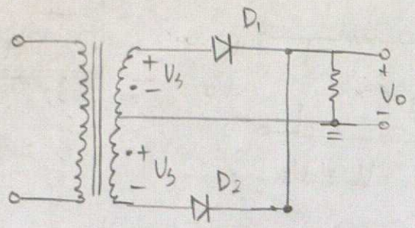
3) 

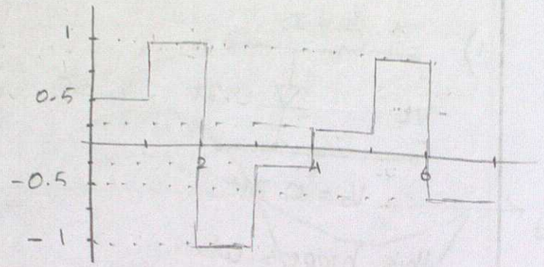
∴ graph c

4)

Problem 2

ideal a)



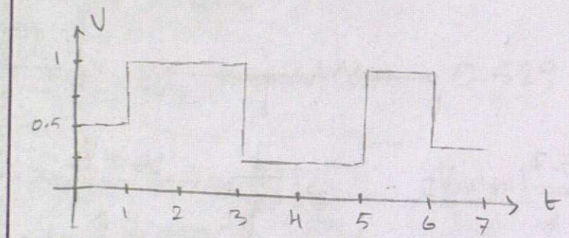


$V_s > 0 \Rightarrow D_1$ ON, D_2 OFF

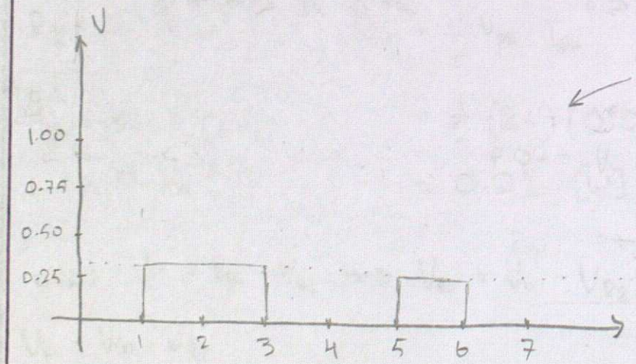
$V_o = V_s$

$V_s < 0 \Rightarrow D_1$ OFF, D_2 ON

$V_o = -V_s$ ← this "V_s" value is negative remember



CUD b)



new case when both diodes are off, meaning V_s had to be b/n -0.7V and 0.7V

0.3V

$V_s > 0.7 \Rightarrow D_1$ ON, D_2 OFF

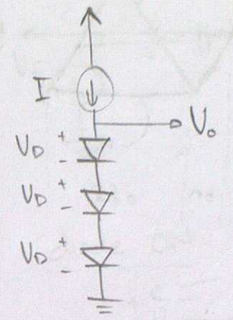
$V_o = V_s - 0.7V$

$V_s < -0.7 \Rightarrow D_1$ OFF, D_2 ON

$V_o = -V_s - 0.7$

Problem 3

$I_s = 10^{-14}$ [A]



① $V_o = 2$ [V] @ room temp, what I?

assume $V_T = 25mV$

$V_o = 3V_D = 2$

$2 = 3V_D = 3V_T \ln(i/I_s)$

$e^{\ln(i/I_s)} = e^{\frac{2}{3V_T}}$

$i = I_s e^{(2/3V_T)} = (10^{-14}) e^{\frac{2}{3(25mV)}} = 3.81mA$

$\therefore I = 3.81mA$

② 1 mA taken away at output, what is change in V_o?

$\Delta V = V_T \ln(i_2/i_1) = (25mV) \ln\left(\frac{2.81mA}{3.81mA}\right) = -8.25\ mV$

↑ this is ΔV for 1 diode, so across 3 diode it is

$\Delta V_o = -0.02$ [V]

③ What is change in V_o when inc. 40°C?

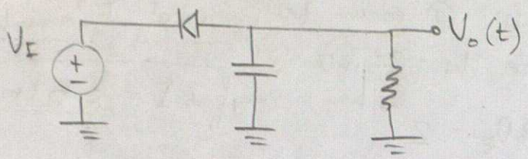
V_D decrease 2mV/°C increase

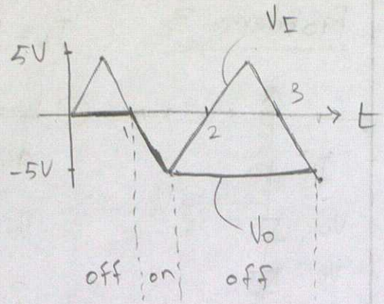
so 40°C increase in temp → 2mV×40 = 80mV dec/diode

3 diodes → 3×80mV = 240mV decreased

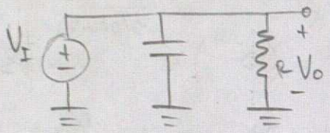
$\therefore \Delta V_o = -240$ [mV]

Problem 4



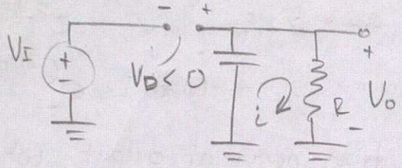


diode is ON



$V_o = V_I$

diode is OFF



$0 < t < 1$: V_I is greater than 0, so diode is off and $V_o = 0$ [V]

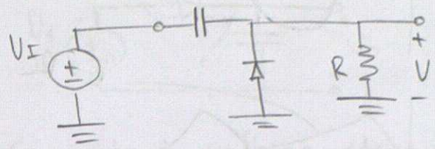
$1 < t < 2$: V_I is negative, so diode is ON, meaning V_o is the same as V_I

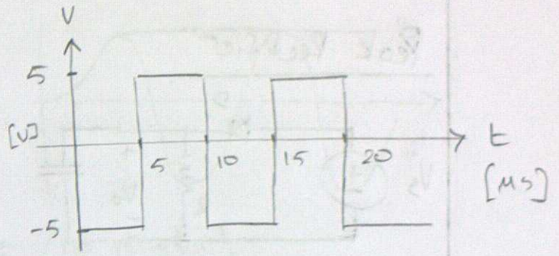
$2 < t < 2$: V_I is positive again, so diode is off, but the capacitor, which was previously charged up to -5V, discharges through R

$$V_o(t) = V_o(\infty) + \left[V_o(1.5ms) - V_o(\infty)\right] e^{-\frac{(t-1.5ms)}{\tau}}$$

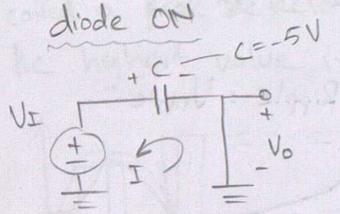
$\tau = (1M)(1m) = 1000s$

Problem 5





diode ON

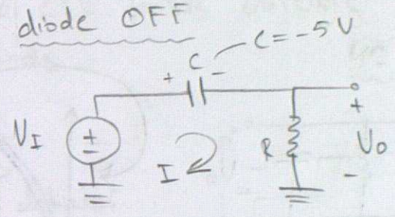


$V_o = 0$

can happen when $V_I < 0$

& charges up: $V_I = V_c$

diode OFF

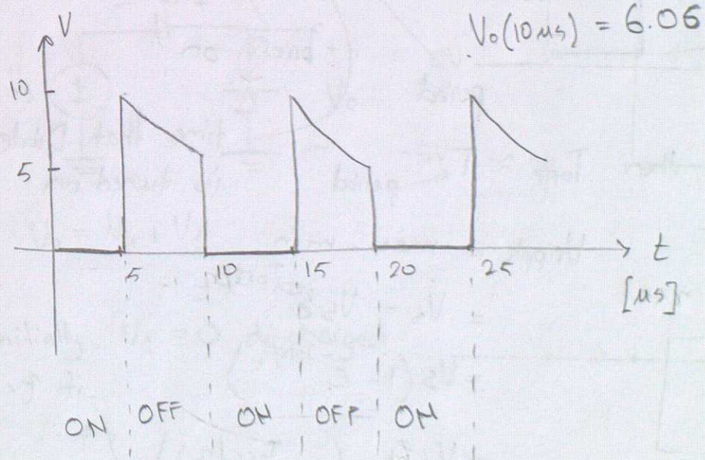


$V_o > 0$

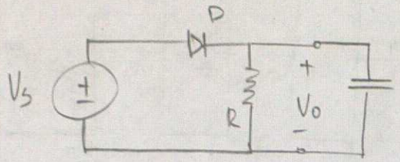
can happen when $V_I > 0$

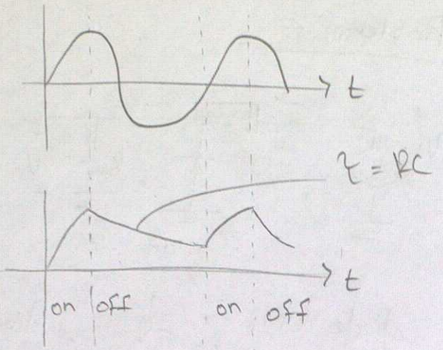
$$V_o(t) = 10\, e^{-\left(\frac{t-5\mu s}{10\mu s}\right)}$$

$V_o(10\mu s) = 6.065$ [V]

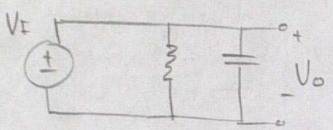


Peak Rectifier

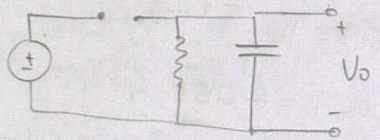


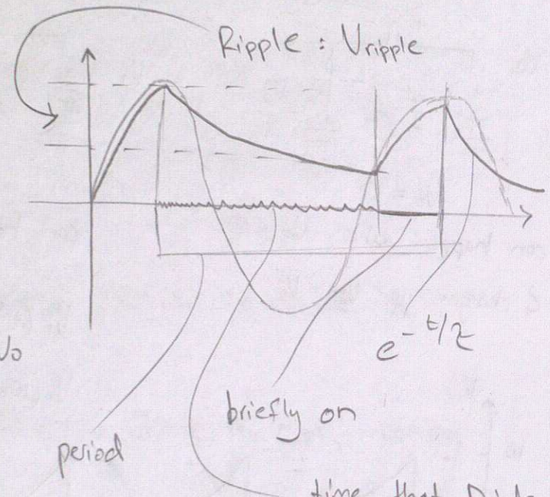


diode ON



diode OFF





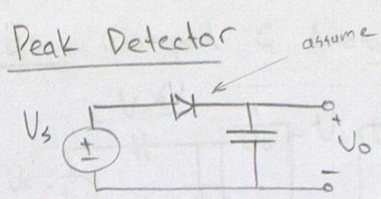
- If ζ is large, then $T_{OFF} \approx T$ ← period — time that Diode is turned on

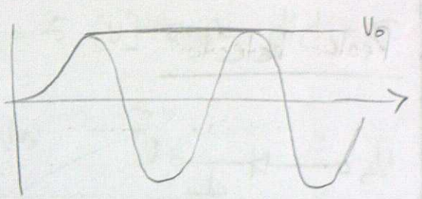
$e^x \approx 1+x$ if $x \ll 1$

$$V_{ripple} \approx \frac{V_{peak}}{fRC}$$

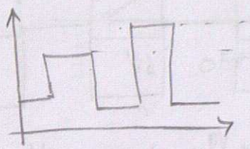
$$\begin{aligned} V_{ripple} &= \text{max} - \text{min} \\ &= V_s - V_s e^{-T_{off}/\tau} \\ &= V_s\left(1 - e^{-T_{off}/\tau}\right) \\ &= V_s\left(1 - (1 - T_{off}/\tau)\right) \quad \text{if } \tau = RC \gg T \\ &= V_s\, T_{off}/\tau \quad \text{(period)} \\ &\approx \frac{V_s T}{\tau} \Rightarrow \frac{V_s T}{RC} \text{ or } \frac{V_s}{fRC} \quad \text{(freq)} \end{aligned}$$

Peak Detector

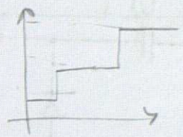




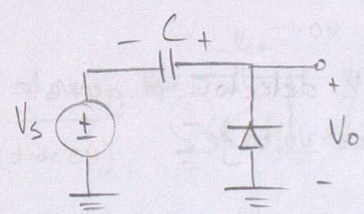
- if no load, voltage stays these (no resistor)
- called a peak detector bc. ckt holds voltage at the highest value it finds

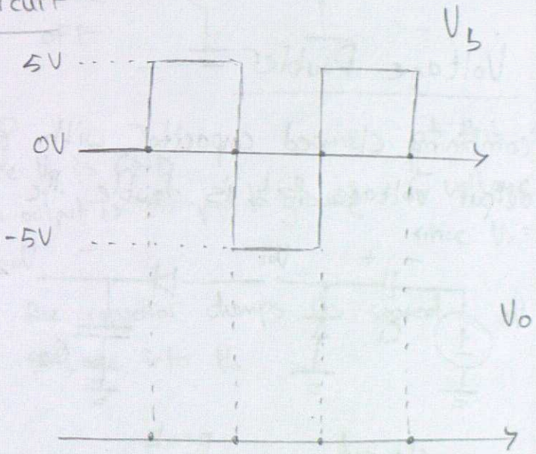


⟹ peak detector



Clamped Capacitor Circuit



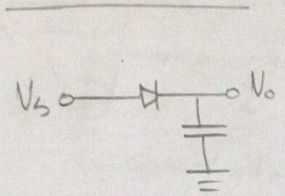


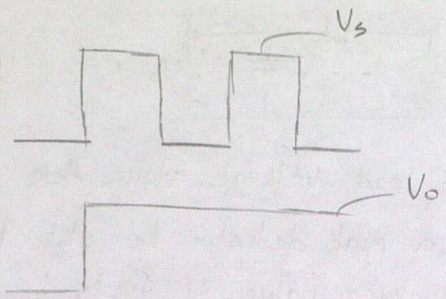
$V_o = V_s + V_c$

- initially, $V_c = 0$ discharged

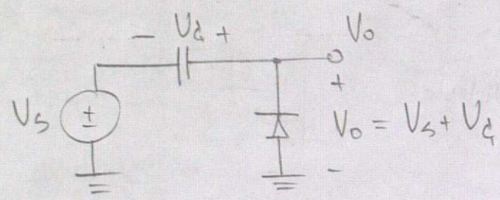
Week 3: Lecture 3 — Sep 20, 2024

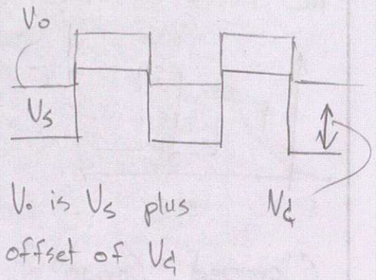
Peak Detector





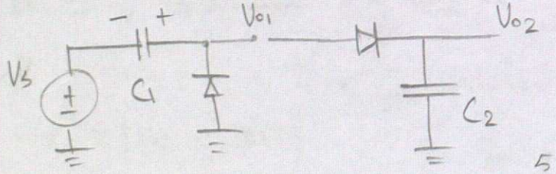
Clamped Capacitor

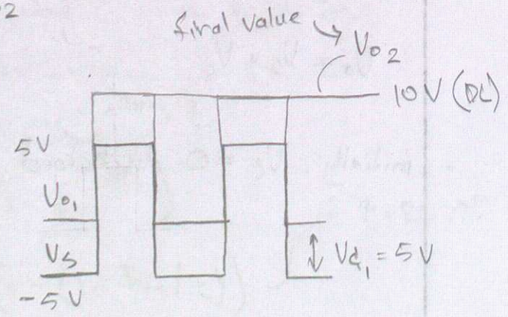




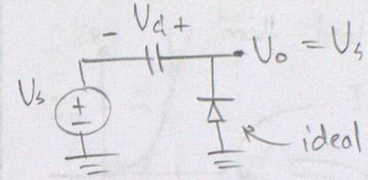
Voltage Doubler

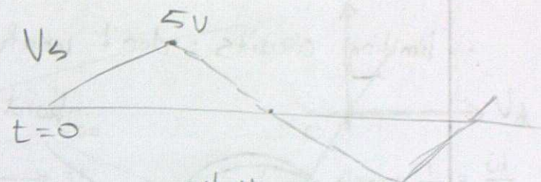
- combining clamped capacitor with peak detector to generate output voltage that is double the peak voltage.

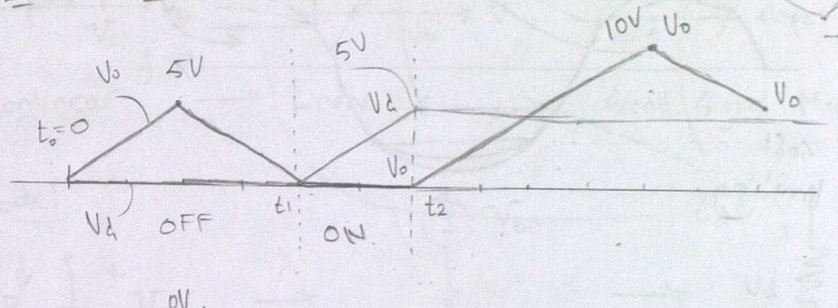




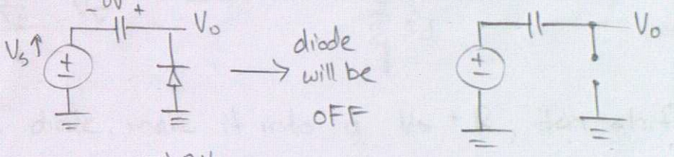
Ex: Clamped C Analysis $V_s = 5$ [V] peak, $V_c = 0$ [V]



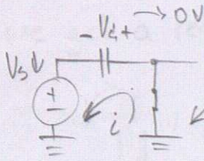




$t_1 = 0$:



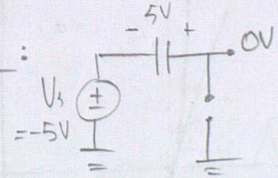
$t = t_1$: (diode ON)



since V_o is GND and output is clamped to ground

at this stage, the C voltage increased since $V_o = V_c + V_s$

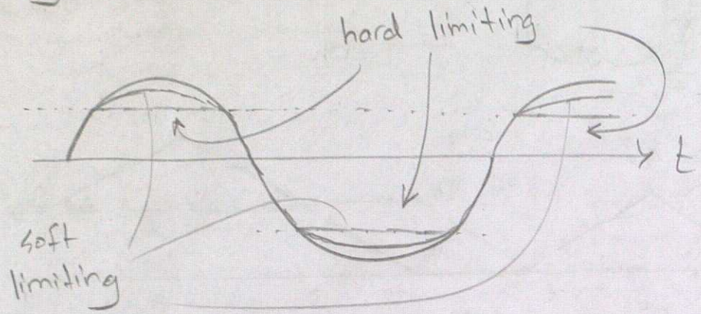
$t = t_2$:



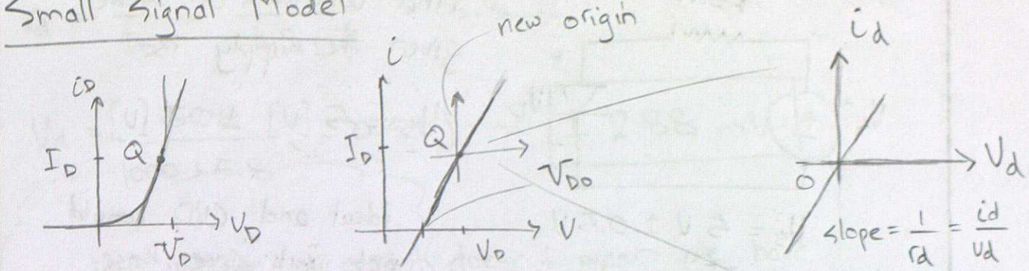
the capacitor dumps its stored voltage into V_o

Hard & Soft Limiting

- limiting circuits: don't want to overload them

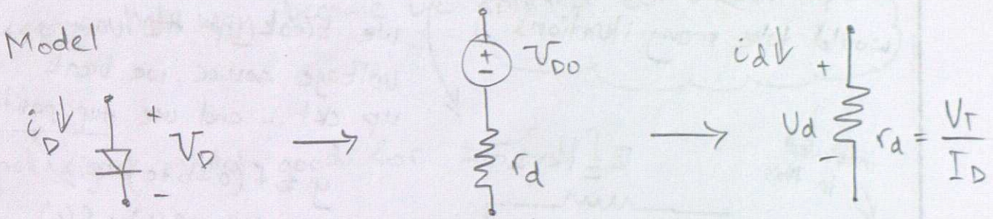


Small Signal Model

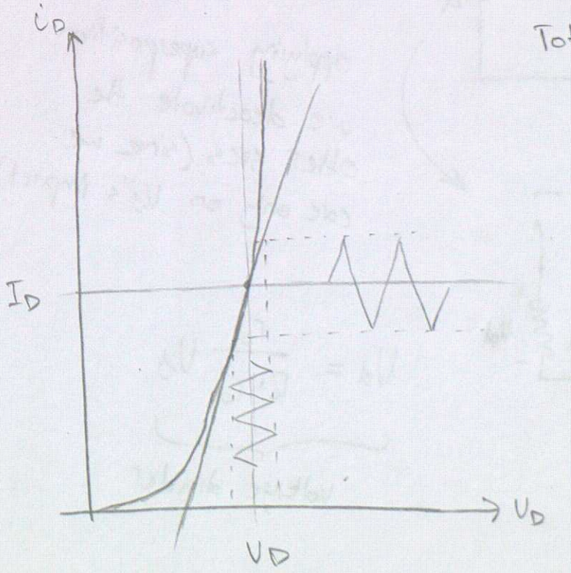


Nonlinear ⟶ Linear ⟶ Small Signal Model

Model



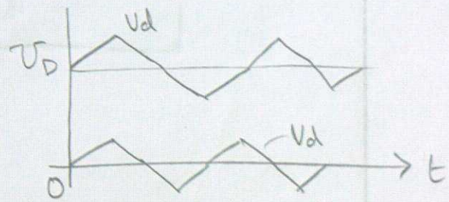
- We take diode, make it into a $V_s + R$, then shift our axes so we get a resistor

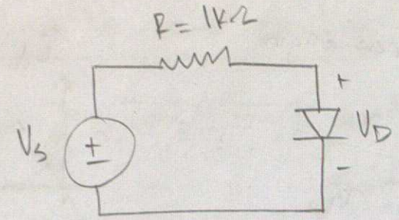


Total signal = DC bias point + small signal

$$V_D = V_D + v_d$$

$$i_D = I_D + i_d$$





$V_s = 5\,V \pm 0.5\,V$

V_s V_s

exponential model would take many iterations

Find variation on diode given the supply is

$V_s = 5\,[V] \pm 0.5\,[V]$

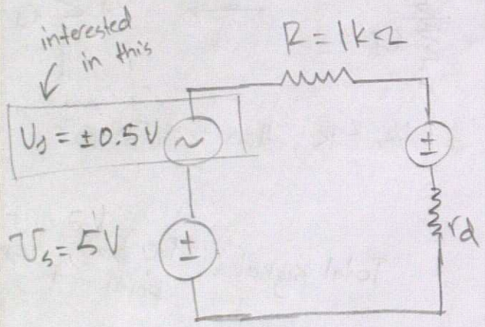
ideal and CVD would not work since those have constant voltage

we break up the varying voltage source, we break up ckt ... and use superposition

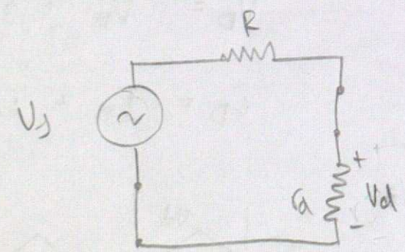
$y = f(a+b+c)$

$y = f(a) + f(b) + f(c)$

interested in this



applying superposition, we deactivate the other srcs (since we care only on V_j's impact)



$$V_d = \underbrace{\frac{r_d}{R + r_d} V_j}$$

Voltage divider

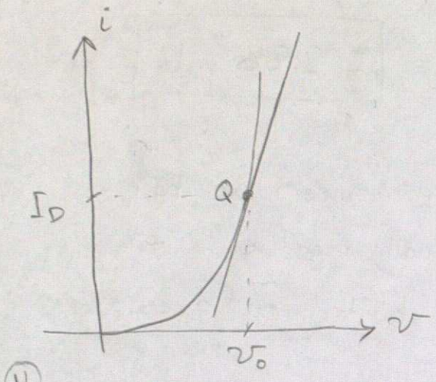
$$r_d = \frac{V_T}{I_D} = \frac{25\,mV}{4.3\,mA} = 5.8\,\Omega$$

$$V_d = \frac{5.8}{1000 + 5.8}\,(\pm 0.5V) = \boxed{\pm 2.88\,mV}$$

negative voltage or current doesn't mean we have leaky diode ⟶ we aren't actually negative ... it seems that way because we shifted our axes.

- small signal model good for $\pm 5\,[mV]$

Deriving $r_d = V_T/I_D$



(i) $i = I_S e^{V/V_T}$

(ii) slope is $\frac{di}{dv}$

(iii) $\frac{di}{dv} = I_S \cdot \frac{1}{V_T} \cdot e^{V/V_T}$

(iv) we want slope @ $V = Q$

(v) $\left.\frac{di}{dv}\right|_Q = \frac{1}{V_T} \cdot \underbrace{I_S e^{V/V_T}}_{I_D} = \frac{I_D}{V_T}$

(vi) since resistance is the inverse of the slope

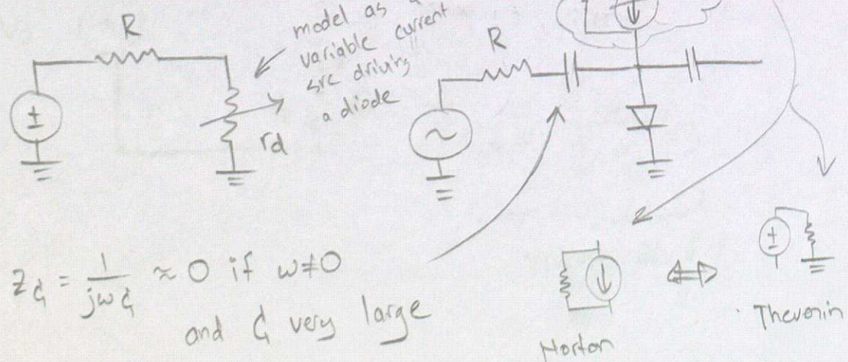
(vii) $r_d = \frac{1}{\text{slope}}$

$$\therefore r_d = \frac{V_T}{I_D}$$ 25 mV

I_D	r_d
10 mA	2.5 Ω
1 mA	25 Ω
0.1 mA	250 Ω

increasing I_D by ten times reduces r_d by ten times

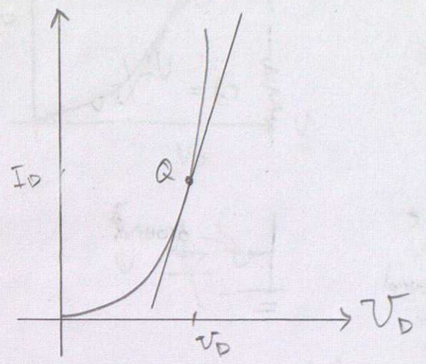
Variable Attenuator



$Z_C = \frac{1}{j\omega C} \approx 0$ if $\omega \neq 0$ and C very large

Small Signal Approx.

- how far can you go before linearization is too inaccurate?



$$e^x = 1 + x + \frac{x^2}{2!} + \frac{x^3}{3!} + \cdots$$

$$\approx 1 + x \quad \text{if } x \gg \frac{x^2}{2!}$$

or $x \ll 2$

$V_D = V_D + v_s$

$$i_D = I_S e^{V_D/V_T}$$

$$= I_S e^{(V_D + v_s)/V_T}$$

$$= \underbrace{I_S e^{V_D/V_T}}_{I_D} \cdot e^{v_s/V_T}$$

$$= I_D \cdot \left(1 + \frac{v_s}{V_T}\right)$$

if $\frac{v_s}{V_T} \gg \frac{\left(\frac{v_s}{V_T}\right)^2}{2!}$

$\frac{v_s}{V_T} \ll 2$

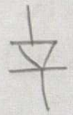
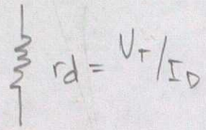
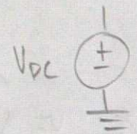
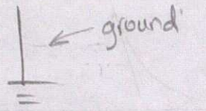
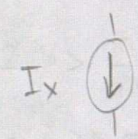
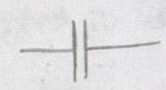
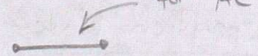
$v_s \ll 2V_T$ ← or 50 mV

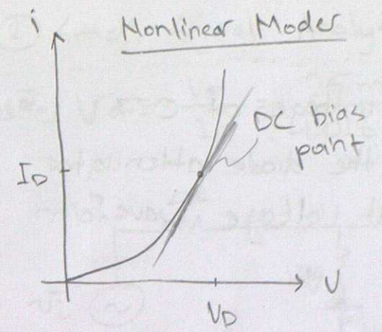
so take $v_s < \frac{1}{10}$ or 5 mV

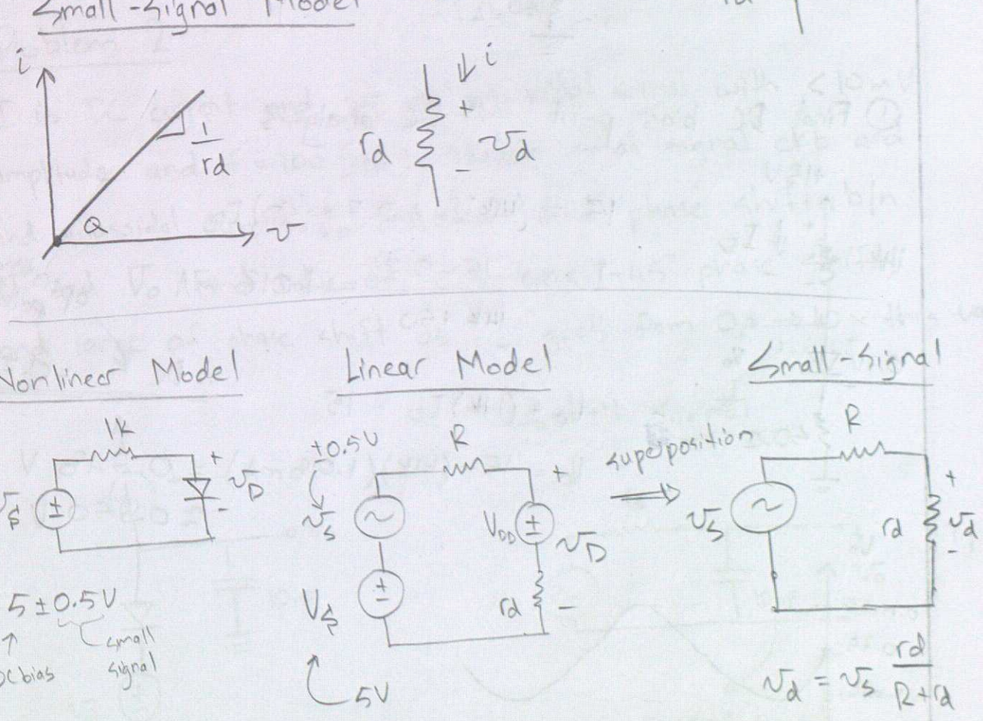
Superposition Notes

- we can remove anything that is not small signal.
- ckt elements have equivalents

Small Signal Model CKt Elements

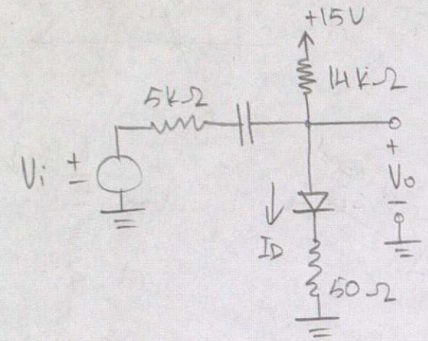
Regular		Small Signal
	diode becomes a resistor	 $r_d = V_T/I_D$
 V_{DC}	constant Voltage source becomes short to ground	 ← ground
	ground is the same	
 I_x	current source becomes open circuit	
 $C \to \infty$ $Z_C = \frac{1}{j\omega C} \to 0$	large capacitor becomes a short circuit in AC	 for AC

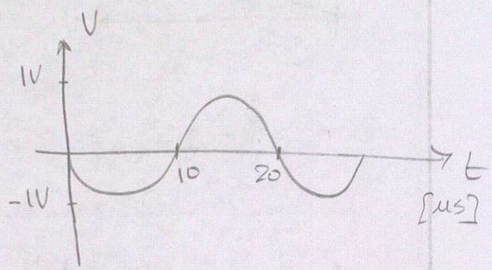




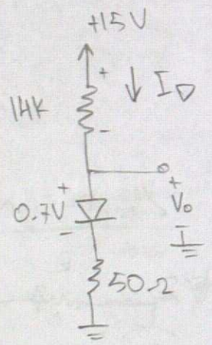
Problem 1

Assume diode has forward bias voltage of 0.7 V when conducting current of 1 mA. For the diode attenuator circuit below, sketch the output voltage waveform





① Find DC bias point → DC analysis



$15 = (14K)I_D + 0.7 + (50)I_D$

$I_D = \frac{15 - 0.7}{14K + 50} = 1.018\ mA$

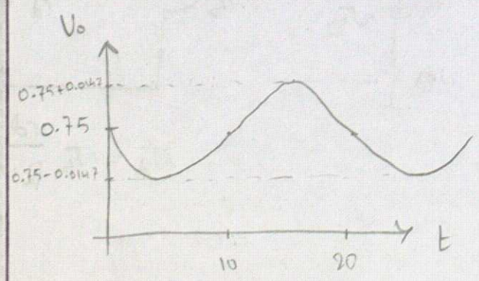
operating point

$\therefore DC = 0.75\ V$

$V_o + (14K)I_D = 15$

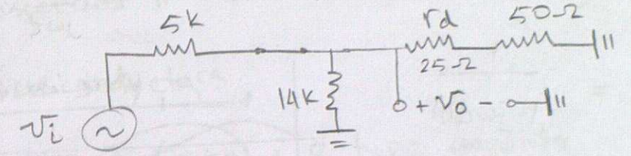
$V_o = 15 - (14K)(1.018mA) = 0.748\ V$

$\simeq 0.750\ V$



② Small Signal Analysis

(a) $r_d = \frac{V_T}{I_D} = \frac{25\ mV}{1.018\ mA} = 25\ \Omega$



$(5K) \leftrightarrow (14K \parallel (rd \leftrightarrow 50))$

$5K \leftrightarrow (14K \parallel 75)$

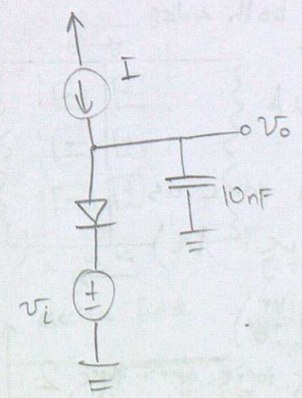
$5K \leftrightarrow 74.6$

Voltage Division : $v_o = v_i \frac{74.6}{74.6 + 5K} = 0.0147\, v_i$

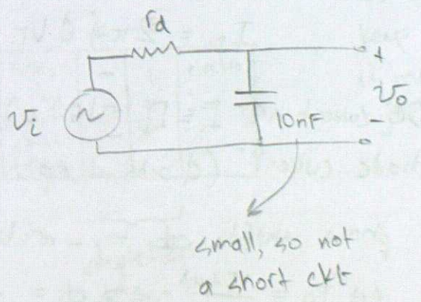
$\therefore V_o = V_o \pm v_o = 0.75 \pm 0.0147$

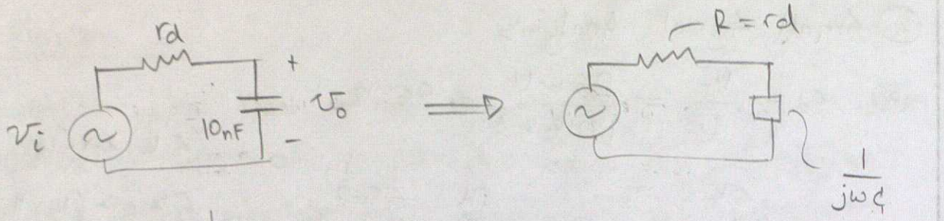
Problem 2

I is DC current and v_i is sinusoidal signal with < 10mV amplitude and f = 100 [kHz]. Sketch small signal ckt and find sinusoidal output V_o and then find phase shift b/n V_i and V_o. Find value of I to have −45° phase shift, and range of phase shift as I goes from 0.1 → 10× this value

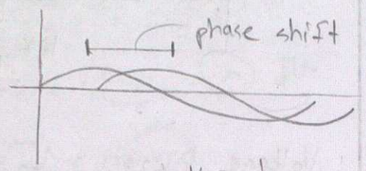


Small Signal





$$\frac{v_o}{v_i} = \frac{\frac{1}{j\omega C}}{r_d + \frac{1}{j\omega C}} = \frac{1}{1 + j\omega C r_d}$$



$\omega = k = \frac{1}{p} =$

$2\pi = p = \frac{1}{f} \Rightarrow 2\pi f = 1$

$$\angle \frac{v_o}{v_i} = \angle \frac{1}{1 + j\omega C r_d}$$

↑ phase shift

$$= \angle(1) - \angle(1 + j\omega C r_d)$$

$$= 0 - \arctan\left(\frac{\omega C r_d}{1}\right)$$

$$= -\arctan(\omega C r_d)$$

$$= -\arctan(2\pi f C r_d) = -45^\circ$$

$\boxed{\omega = 2\pi f}$

set equal to -45° as per question

$$\arctan\left(2\pi f C \frac{V_T}{I_D}\right) = 45^\circ$$

take tan of both sides

$$2\pi f C \frac{V_T}{I_D} = 1$$

$$I_D = 2\pi f C V_T = 157\,\mu A$$

DC current src $I = I_D = 157\,\mu A$ since it's same as diode current (C acts a open ckt since we in DC)

phase shift $\phi = -\arctan\left(2\pi f C \frac{V_T}{I_D}\right)$

set $I_D = \frac{157\,\mu A}{10} \Rightarrow \phi = -84.3^\circ$

set $I_D = 157\,\mu A \times 10 \Rightarrow \phi = -5.71^\circ$

} range from these 2

pn Junction

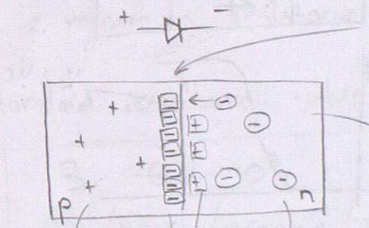
- used in more complex semiconductor devices (eg. transistors)
- discovered in Bell Labs, 1940 during WW II

Semiconductors

→ group 3 (Boron) : p-type dopants

→ group 5 (Phosphorus): n-type dopants

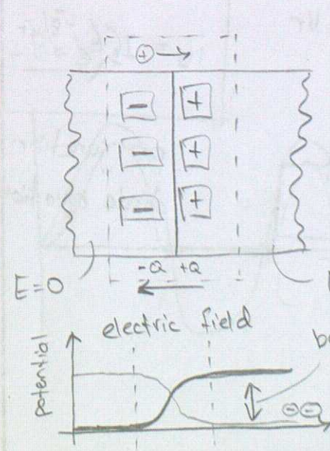
pn Junction



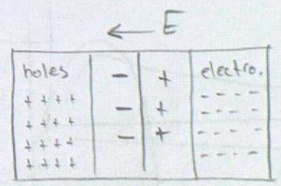
at the interface, electrons pass and find a spot in a hole

when you take away electrons from this side, you "uncover" a positive charge

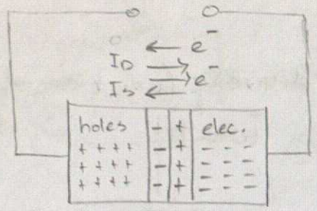
positive charges fixed (revealed after e^- hops)



the dipole at the interface creates an electric field

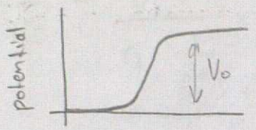


as electrons keep hopping, it makes "hill" higher, so new electrons in n-region can't "climb hill"

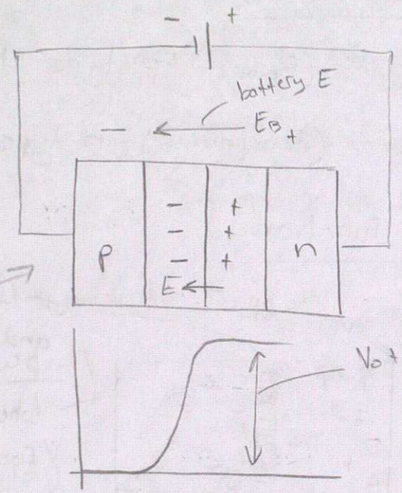


I_D: diffusion current

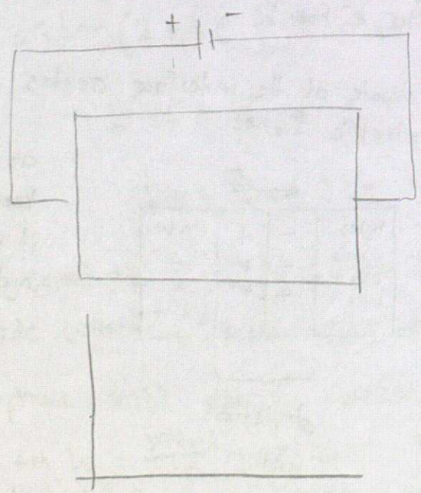
I_S: drift current

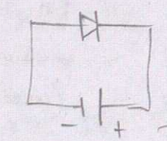


open:



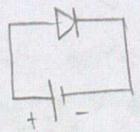
the battery's electric field basically aids the existing E inside the interface region, making it harder for electrons to flow "backward"





$$i_D = I_S\left(e^{V_D/V_T} - 1\right)$$

pn junction diode equation



PE1

c) $V_{ripple} \approx \frac{V_{peak}}{fRC}$

Q: What is minimum R for the ripple voltage V_{ripple} to be no greater than 0.5 V?

$V_{peak} = 2.5\ V$, $f = 1000\ Hz$, $C = 100\ nF$

$V_{ripple} \leq 0.5\ V$

$0.5 \geq \frac{V_{peak}}{fRC}$ $\quad -0.7V$

$R \geq \frac{V_{peak}}{0.5fC} = \frac{2.5 - 0.7}{0.5(1000)\times(100\times10^{-9})} = 36000 = 36k\Omega$

$\therefore$ minimum resistance is $\boxed{R = 36k\Omega}$

d) standard resistance value:

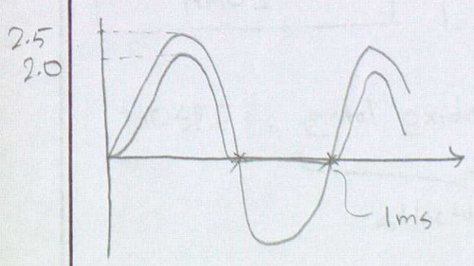
	3	6	10^3	2%
①	orange	blue	orange	red

ideally, we should pick a resistor of less than 36kΩ

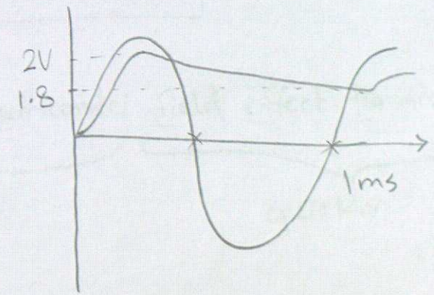
LTspice V_{ripple}: $(2.008721) - (1.7132858) = 0.295 < 0.5$

411 mV < 0.5

PE1a)

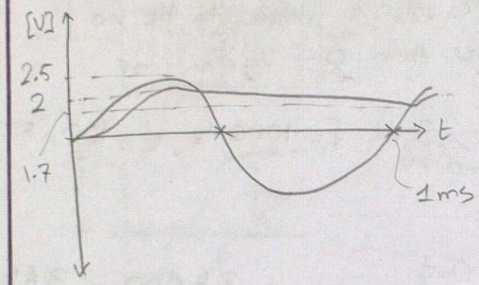


PE1b)



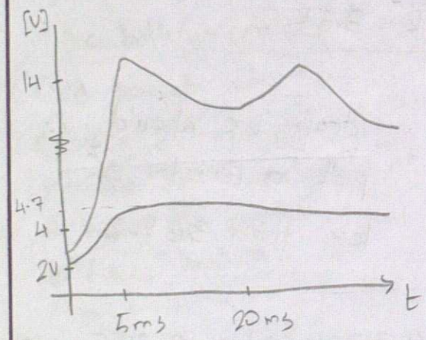
PE1c) estimated $R = 36\,k\Omega$ (calculated)

PE1d) minimum value of R: ① 36 kΩ ②



ripple voltage (simulated) ≈ 1.326 mV

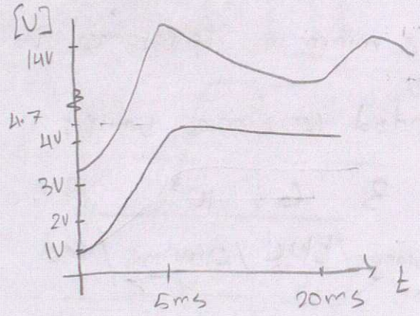
PE2 a)



PE2b) $(V_{out})_{avg} = 4.7V$

$V_{ripple} = 1.326V$

PE2c)

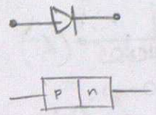


PE2c) $(V_{out})_{avg} = 4.7V$

$V_{ripple} = 1.36V$

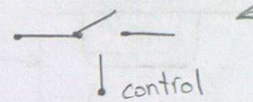
Transistor

Diodes



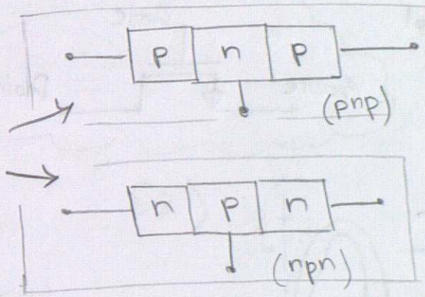
2-terminal device, decides for itself

Switch ← transistor



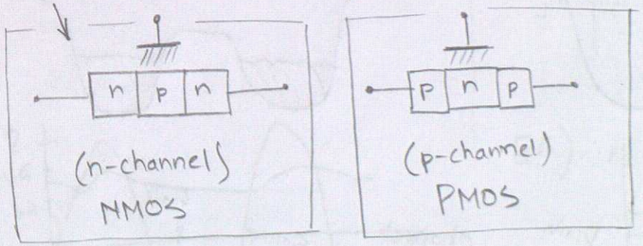
3-terminal device

bipolar junction transistor (BJT)



2 ways to create 3-terminal device using pn junctions

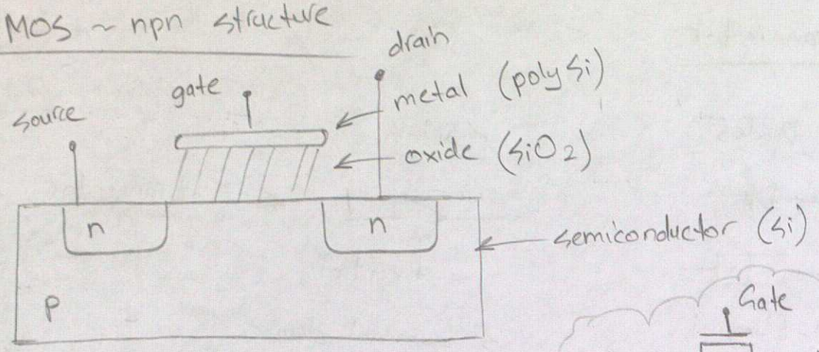
MOSFET



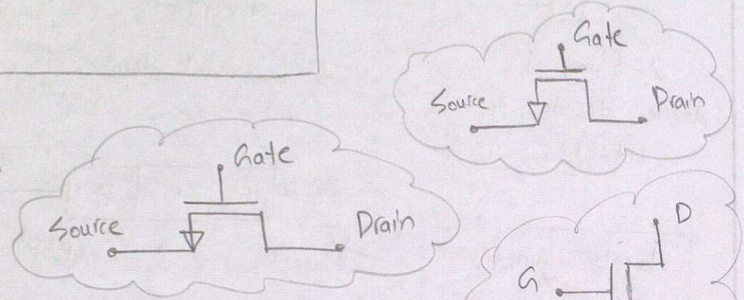
MOSFET: metal oxide semiconder field effect transistor

structure — operation

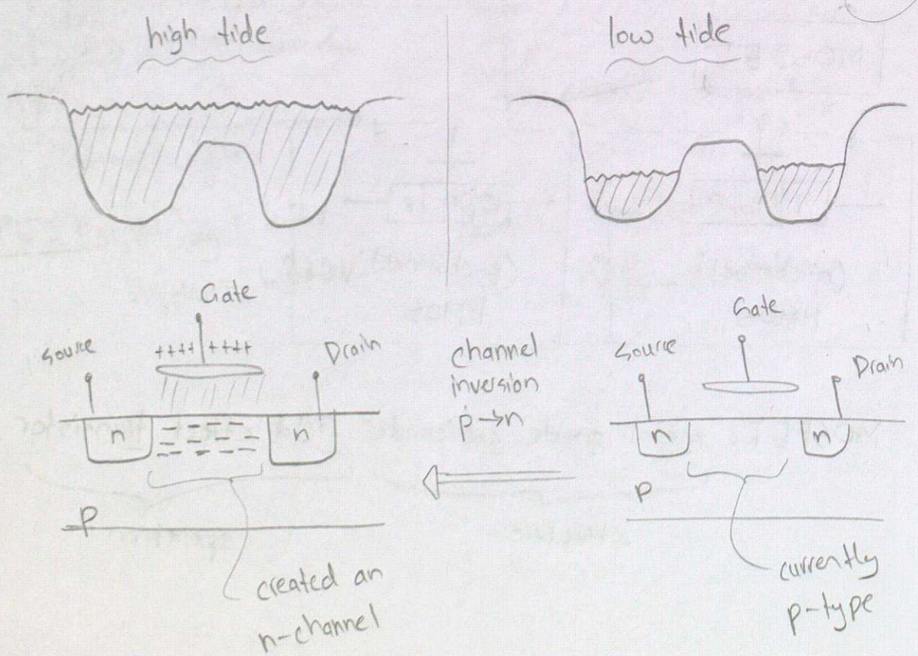
NMOS ~ npn structure



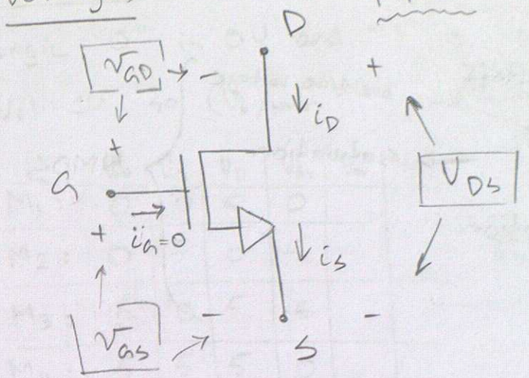
Ckt Symbol



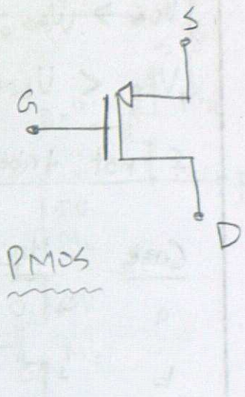
Operation



Voltages



$i_G = 0$ since gate is a capacitor

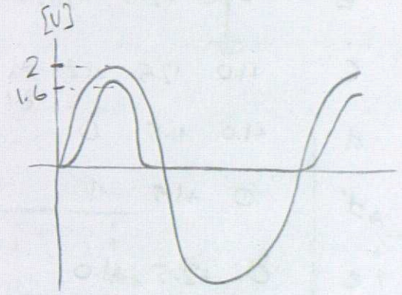


Lab 2

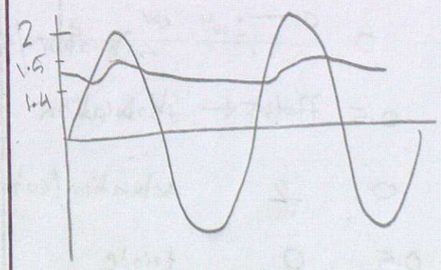
E1)

a	b	o
0	0	0
0	1	1
1	0	1
1	1	1

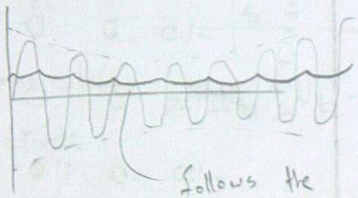
E2)



E3)



E4)



follows the waveform of the low frequency modulation

Tutorial 4 — Oct 2, 2024

Summary

"$V_{GS} = V_G - V_S$"

$\begin{cases} V_{GS} > V_t \longrightarrow \text{not cutoff} \\ V_{DS} > V_{GS} - V_t = |V_{ov}| \longrightarrow \text{saturation} \\ V_{GD} < V_t \Longrightarrow \text{saturation} \end{cases}$ NMOS

(overdrive voltage)

if not, triode

Case	V_S	V_G	V_D	V_{GS}	V_{ov}	V_{DS}	Region
a	+1.0	+1	+2	1-1=0	0-1=-1	2-1=1	cutoff
b	+1.0	+2.5	+2.0	2.5-1=1.5	1.5-1=0.5	2-1=1	saturation
c	+1.0	+2.5	+1.5	1.5	0.5	0.5	saturation/triode
d	+1.0	+1.5	0	0.5	-0.5	-1	saturation*
d'	0	+1.5	+1	1.5	0.5	1	saturation
e	0	+2.5	+1.0	2.5	1.5	1	triode
f	+1.0	+1.0	+1.0	0	-1	0	cutoff
g	-1.0	0	0	1	0	1	saturation/cutoff
h	-1.5	0	0	1.5	0.5	1.5	saturation
i	-1.0	0	+1.0	1	0	2	saturation/cutoff
j	+0.5	+2.0	+0.5	1.5	0.5	0	triode

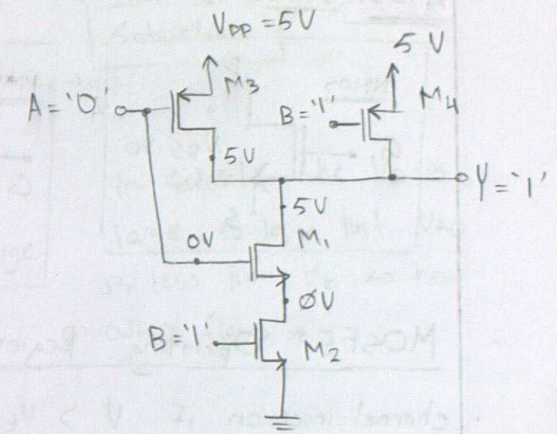
flip drain and source if negative →

Problem 1

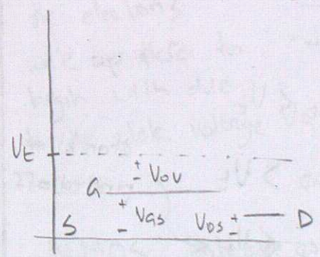
Logic "0" is 0V and "1" is $V_{DD} = 5V$

$|V_t| = 1V$, so $(V_t)_{NMOS} = +1$ $(V_t)_{PMOS} = -1$

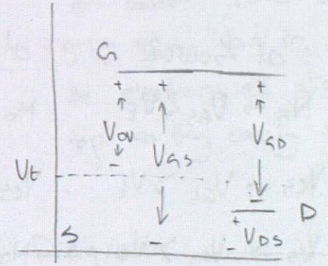
	V_S	V_G	V_D	V_{GS}	V_{ov}	V_{DS}
M_1:	0	0	5	0		
M_2:	0	5	0	5		
M_3:	5	0	5	-5		
M_4:	5	5	5	0		



NMOS Operation Regions

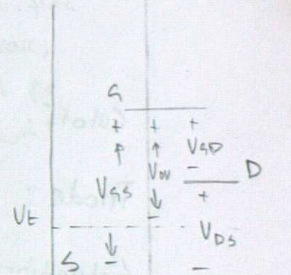


$V_{GS} < V_t \rightarrow$ cutoff



$V_{GS} > V_t \rightarrow$ not cutoff

$V_{DS} < V_t \rightarrow$ triode

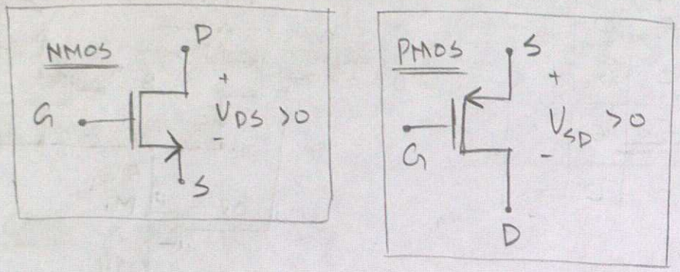


$V_{GS} > V_t \rightarrow$ not cutoff

Week 5: Lecture 2 — Oct. 2, 2024

Source and Drain Convention

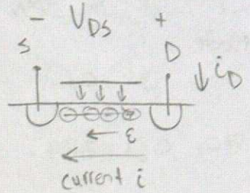
- NMOS: source is terminal at lower voltage (compared to Drain)
- PMOS: source is terminal at higher voltage

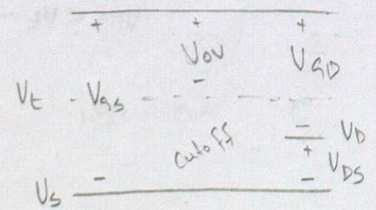


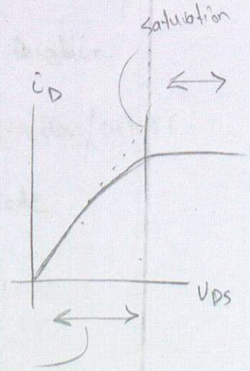
MOSFET Operating Regions

- channel inversion if $V > V_t$ threshold voltage
- do we have channel inversion?

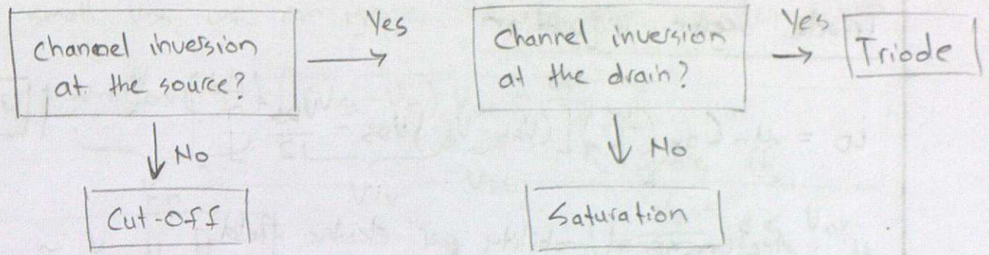
	at Source	at Drain
Cutoff:	No → $V_{GS} < V_t$	No → $V_{GD} < V_t$
Triode:	Yes → $V_{GS} > V_t$	Yes → $V_{GD} > V_t$
Saturation:	Yes → $V_{GS} > V_t$	No → $V_{GD} \ll V_t$ ← channel is pinched off



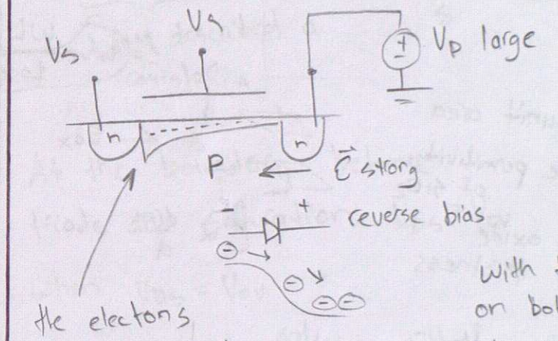




increasing V_D means decreasing V_{GD}



Week 5: Lecture 3



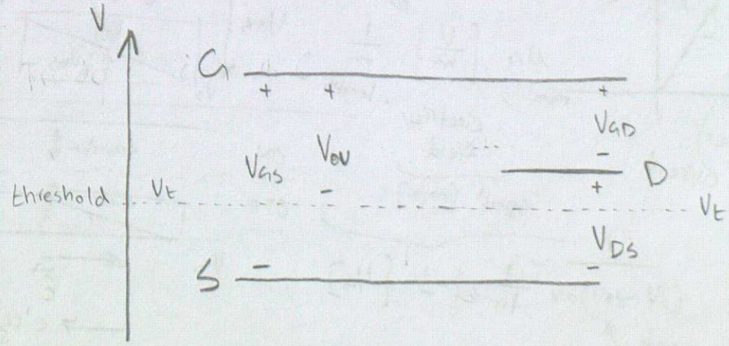
the electrons were up there to begin with due to the plate voltage V_S

in saturation, the V_D is large, so large that V_{GD} is less than V_t, so now current flows

with the normal diode, electrons on bottom have a hard time going up... but in this case, the electrons are already at the top, so they easily fall down

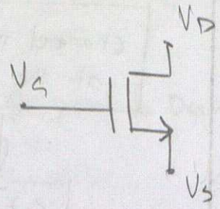
NMOS Voltage level Diagram

$V_{DS} < V_t$: cutoff



Triode Region Equation

$$i_D = \mu_n C_{ox} \left(\frac{W}{L}\right)\left[(V_{GS} - V_t)V_{DS} - \frac{V_{DS}^2}{2}\right]$$



μ_n: electon speed/mobility per electric field

$$\mu_n = \frac{\text{speed}}{\text{electric field}} \quad [=] \quad \frac{m/s}{V/m}$$

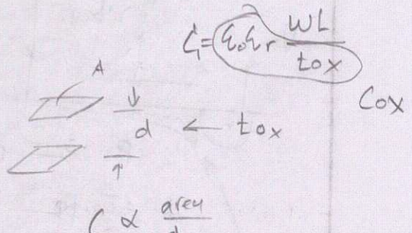
V_t: threshold voltage

C_{ox}: gate capacitance per unit area

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$

ε_{ox} ← relative permitivity of SiO_2

t_{ox} ← gate oxide thickness



$$i_D = C_{ox}(W \times L)\left[V_{GS} - V_t - \frac{V_{DS}}{2}\right]\mu_n \cdot \frac{V_{DS}}{L} \cdot \frac{1}{L}$$

C — "capacitor voltage" effective voltage, V — charge Q

effective voltage: $V_{GS} - V_t - \frac{1}{2}V_{DS}$

$$i_D = Q \cdot \frac{1}{s}$$

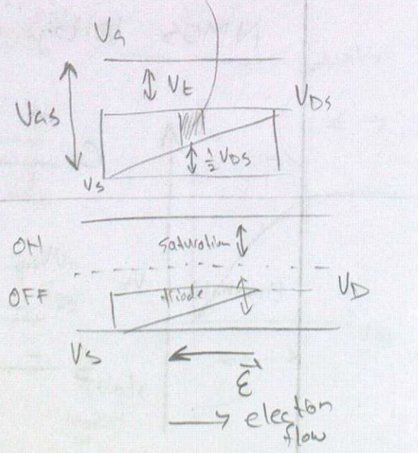
coulombs per second ≡ current

μ_n mobility $\left[\frac{U}{m}\right]$ $\frac{1}{m}$ length

electric field

speed [m/s]

$\frac{1}{\text{time}}$ [=] $[1/s]$



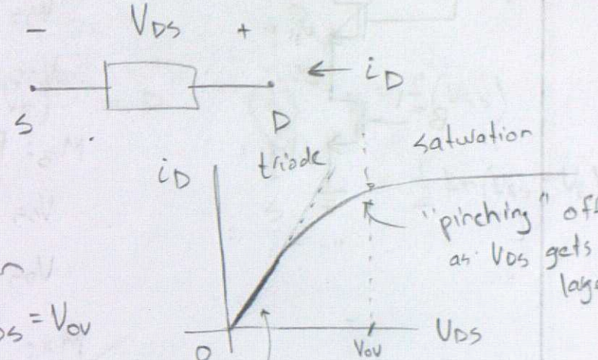
for small V_{DS}, we can ignore the squared V_{DS} term

$$i_D = \underbrace{\mu_n C_{ox}\left(\frac{W}{L}\right)}_{K_n}\left[\underbrace{(V_{GS} - V_t)}_{V_{OV}}\underbrace{V_{DS}}_{V_{DS}} - \frac{V_{DS}^2}{2}\right]$$

ignore if $\frac{V_{DS}^2}{2} \ll V_{OV}$

$$i_D \approx K_n V_{OV} V_{DS}$$

$i_D \propto V_{DS}$ — just described a resistor



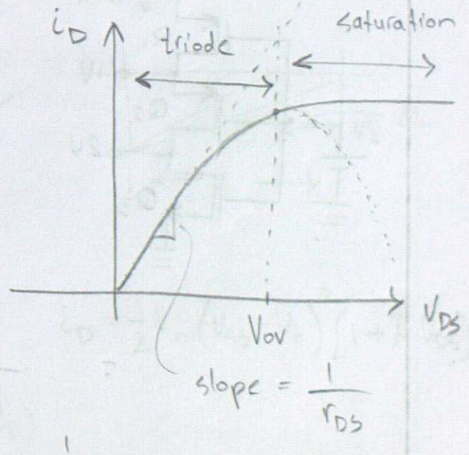
At the boundary between triode and saturation: $V_{DS} = V_{OV}$

when $V_{DS} = V_{OV}$

$$i_D = k_n\left(V_{OV}V_{DS} - \frac{V_{DS}^2}{2}\right)$$

$$= k_n\left(V_{OV}^2 - \frac{V_{OV}^2}{2}\right)$$

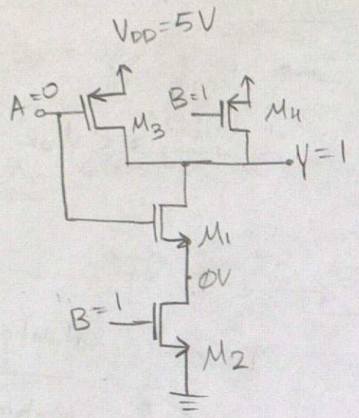
$$= \frac{1}{2}k_n V_{OV}^2$$



$$r = \frac{1}{k_n(V_{GS} - V_t)}$$

V_{GS}

Problem 1



M_1: NMOS cutoff

$V_{GS} = 5-5 = 0 < V_t = 1$

M_2: NMOS triode

$V_{GS} = 5-0 = 5 > V_t$, not cutoff

$V_{GD} = 5-0 = 5 > V_t$, triode

M_3: PMOS triode

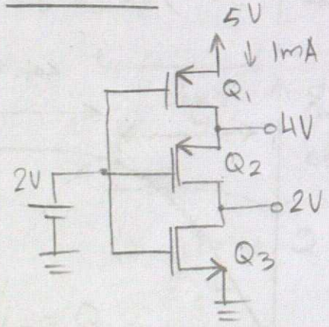
$V_{SG} = 5-0 = 5 > |V_t|$, not cutoff

$V_{DG} = 5-0 = 5 > |V_t|$, triode

M_4: PMOS cutoff

$V_{SG} = 5-5 = 0 < |V_t|$, cutoff

Problem 2



Q_1: PMOS, triode

$V_{SG} = 5-2 = 3 > V_t$, not cutoff

$V_{DG} = 4-2 = 2 > V_t$, triode

Q_2: PMOS, saturation

$V_{SG} = 4-2 = 2 > V_t$, not cutoff

$V_{DG} = 2-2 = 0 < V_t$, saturation

Q_3: NMOS, saturation

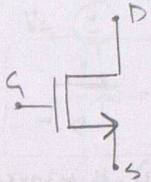
$V_{GS} = 2-0 = 2 > V_t$, not cutoff

$V_{GD} = 2-2 = 0 < V_t$, saturation

Saturation Region

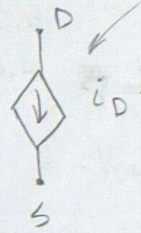
pinchoff state, $V_{DS} = V_{OV}$

$$i_D = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right) (V_{GS} - V_{tn})^2 [1 + \lambda V_{DS}]$$



Saturation

$$i_D = \frac{1}{2} k_n (V_{GS} - V_t)^2$$



Voltage-controlled current source

$$i_D = f(V_{GS}) = \frac{1}{2} k_n (V_{GS} - V_t)^2$$

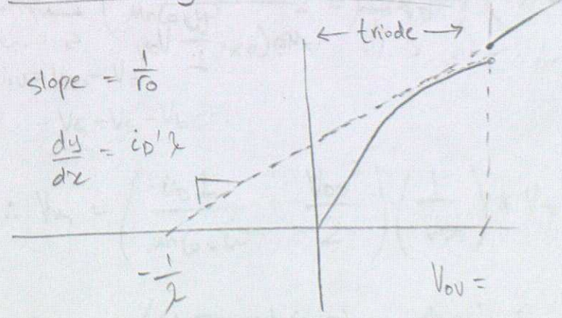
Modeling MOSFET

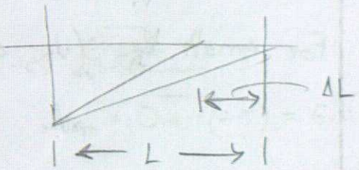
1) cutoff → open circuit

2) triode → resistor (V_{GS}-controlled) S ⎓ D

3) saturation → current source (V_{GS}-controlled)

Channel-length Modulation





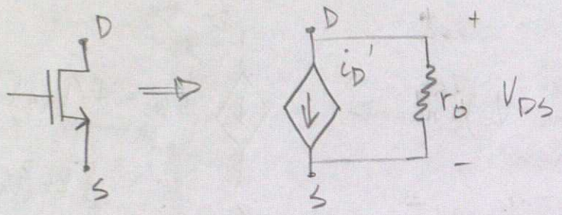
$$i_D = \frac{1}{2} k_n (V_{GS} - V_t)^2 [1 + \lambda V_{DS}]$$

$$i_D = \underbrace{\frac{1}{2} k_n (V_{GS} - V_t)^2}\ [1 + \lambda V_{DS}]$$

i_D' = drain current without channel length modulation

$= i_D' + i_D' \lambda V_{DS} \longrightarrow i_D' \lambda V_{DS}$

$1/r_O$



$$r_O = \frac{1}{i_D' \lambda}$$

output resistance in saturation

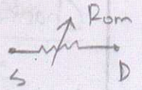
NMOS Summary

In cutoff region: $I_D = 0 \leftarrow (V_{GS} < V_t)$

In triode region: $I_D = \mu_n C_{ox} \frac{W}{L} (V_{ov} V_{DS} - \frac{1}{2} V_{DS}^2) \leftarrow \begin{pmatrix} V_{GS} > V_t \\ V_{GD} > V_t \end{pmatrix}$

In saturation region: $I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} V_{ov}^2 \leftarrow (V_{GS} > V_t,\ V_{GD} \leq V_t)$

For small V_{DS}, $(V_{DS} \ll 2V_{ov}) \rightarrow R_{on} = \frac{1}{\mu_n C_{ox} \frac{W}{L} V_{ov}}$



Tutorial 4

Problem 3

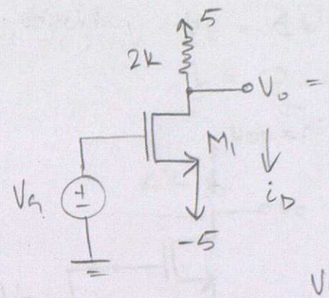
Find V_G for $V_O = -4.5$ [V], M_1 in triode,

$V_{DD} = 5$ V $\mu_n C_{ox} = 50 \frac{\mu A}{V^2}$

$V_{SS} = 5$ V $\frac{W}{L} = \frac{20}{0.5}$

$R_D = 2$ kΩ

$V_t = 0.4$ $\lambda = 0$



M_1 : NMOS, triode

$V_{GS} > V_t = 0.4$

$V_{GD} > V_t = 0.4 \equiv V_{DS} < V_{ov}$

$$i_D = \mu_n C_{ox} \frac{W}{L} \left(\overbrace{(V_{GS} - V_t)}^{V_{ov}} V_{DS} - \frac{V_{DS}^2}{2} \right)$$

$$i_D = \frac{5 - (-4.5)}{2k} = 4.75 \text{ mA}$$

$$i_D = \mu_n C_{ox} \frac{W}{L} \left(V_{ov} V_{DS} - \frac{V_{DS}^2}{2} \right)$$

$$V_{ov} V_{DS} - \frac{V_{DS}^2}{2} = \frac{i_D L}{\mu_n C_{ox} W}$$

$$V_{ov} = \left(\frac{i_D L}{\mu_n C_{ox} W} + \frac{V_{DS}^2}{2} \right) \left(\frac{1}{V_{DS}} \right)$$

$V_{ov} = V_{GS} - V_t$

$= V_G - V_S - V_t$

$$\therefore V_G = \left(\frac{i_D L}{\mu_n C_{ox} W} + \frac{V_{DS}^2}{2} \right) \left(\frac{1}{V_{DS}} \right) + V_S + V_t$$

$$V_G = \left(\frac{(4.75\text{mA})(0.5)}{(50 \times 10^{-6})(20)} + \frac{(0.5)^2}{2} \right) \left(\frac{1}{(0.5)} \right) + (-5) + (0.4)$$

$V_{DS} = -4.5 - (-5) = \frac{1}{2}$ V

$10 < V_{ov}$

$10 < V_{GS} - V_t$

$10 + 0.4 < V_{GS}$

$V_{GS} > 10.4$

$\boxed{V_G = 0.4 \text{ V}}$ ✓

Check

$V_{GS} = 0.4 - (-5) = 5.4 > V_t$

not cutoff ✓

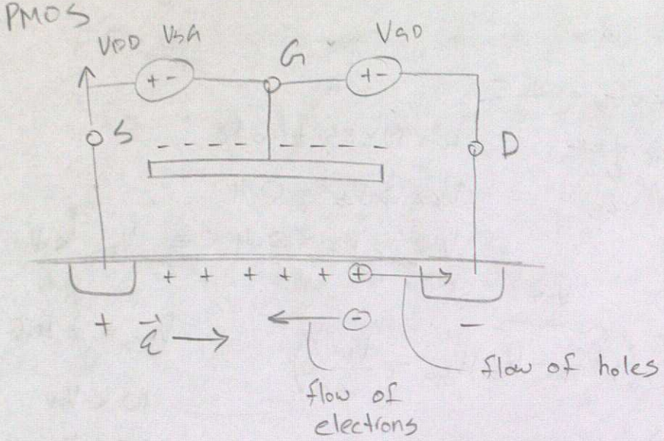
$V_{GD} = 0.4 - (-4.5) = 4.9 > V_t$

triode ✓

Week 6: Lecture 2 Oct 9, 2024

Analysis MOSFET DC

PMOS



- electron mobility is 2-3 higher than hole mobility (holes move slower)
- treat electrons as positively charged things for PMOS

Rules for Ckt Analysis

1) Rules for the ckt themselves (KVL, KCL)
2) Rules for ckt elements
   - resistors : V=IR
   - diodes — ideal, CVD, exponential
   - MOSFETS — cutoff, triode, saturation

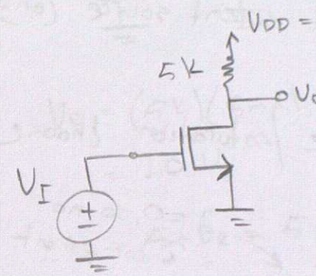
Process: Assume → Analyze → Verify

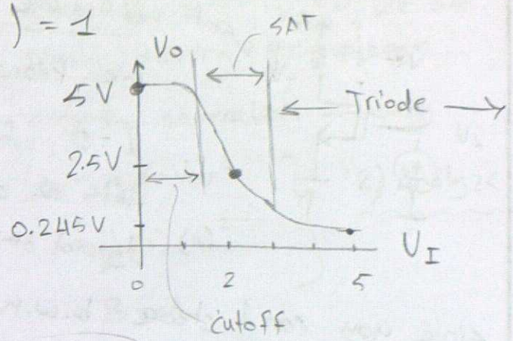
Ex 1 Find output V when input is 0V, 2V, 5V

Assume: $k_n = \mu_n C_{ox} (\frac{W}{L}) = 1$

$V_t = 1V$

$\lambda = 0$

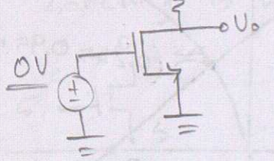




NOT Gate

amplifier

Case 1: V_i = 0V, $V_o = 5$ [V]

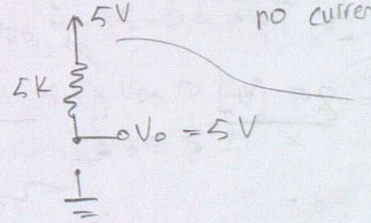


1) Assume

$V_{GS} = 0$, no current

$V_{GS} = 0V$, cutoff

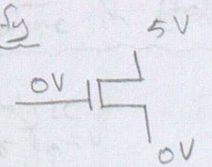
2) Analyze



no current, so $V_o = 5V$

pullup resistor, since output gets "pulled" up to 5V when switch is OFF

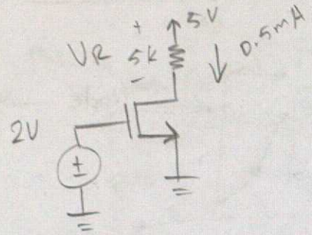
3) Verify



$V_{GS} = 0 < V_t$, cutoff

no current ✓ verified

Case 2: $V_i = 2V$



1) Assume

we know $V_{GS} = 2 > V_t$, so no cutoff

$\lambda = 0$, which means in saturation, it acts as a perfect current source (only depend on V_{GS})

since you can't choose b.w.n triode / saturation, choose saturation

2) Analyze $i_D = \frac{1}{2} k_n (V_{GS} - V_t)^2$ ← $\lambda = 0$, so no λ component

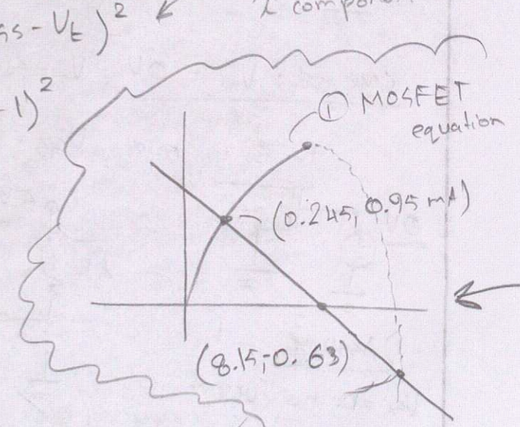
$= \frac{1}{2}(1)(2-1)^2$

$= \frac{1}{2}$ mA

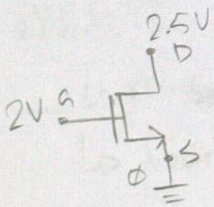
$V_R = (5V)(0.5mA)$

$= 2.5V$

$\therefore V_o = 5 - 2.5 = \underline{2.5\ [V]}$



3) Verify



$V_{GS} = 2 > V_t$, not cutoff ✓

$V_{DS} = 2.5 - 0 = 2.5$

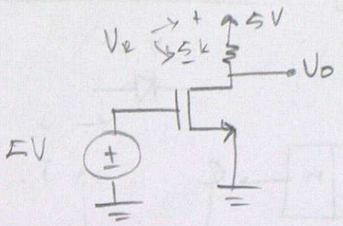
$V_{OV} = 2V - 1V = 1V$

since $V_{DS} = 2.5 > V_{OV} = 1V$

saturation mode ✓

assumption verified

Case 3: $V_i = 5V$



$V_R = (5k)(8mA)$

$= 40V$

$\therefore V_o = 5 - V_R = 5 - 40 = \underline{-35V}$

doesn't make sense, since you can't generate $-35V$ with 1 pos source all at ounce

1) Assume

since $V_{ov} = 5 - 1 = 4V$, we are really driving the voltage

- assume saturation — easy

$i_D = \frac{1}{2} k_n V_{ov}^2$

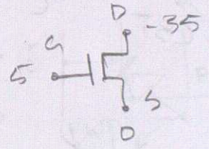
$= \frac{1}{2}(1)(4)^2$

$= 8$ mA

2) Analyze

3) Verify

"something is wrong"



$V_{DS} = -35 - 0 = -35$ [V]

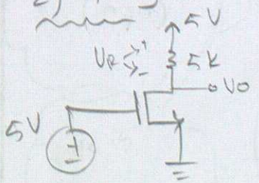
in sat, $V_{DS} > V_{ov}$

$-35 \not> 1$ ✗ this is wrong

∴ not in saturation

1) Assume in triode since it's ON and not saturation (only option)

2) Analyze



$i_D = k_n\left(V_{ov} V_{DS} - \frac{V_{DS}^2}{2}\right)$ ← the parabolic component from MOSFET

$i_D = (1)\left((4)V_o - \frac{V_o^2}{2}\right)$ ← equation 1

$V_o = V_{DD} - V_R$

$V_o = V_{DD} - i_D R_D$

$V_o = 5 - i_D(5k)$ ← equation 2 from KVL

$V_{DS} = V_o$ ← the linear component

$V_o = 5 - \left(4V_o - \frac{V_o^2}{2}\right)(5k)$

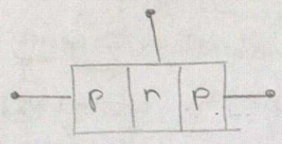
solving: $V_o = \underline{8.15}$ V or $\underline{0.245}$ V

8.15 wrong, since that's greater than 5V

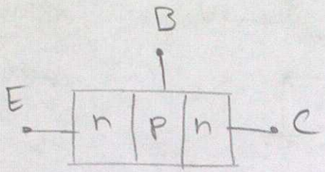
0.245 correct

Week 6: Lecture 3 — Oct 11, 2024

Intro. to BJT's — bipolar junction transistor

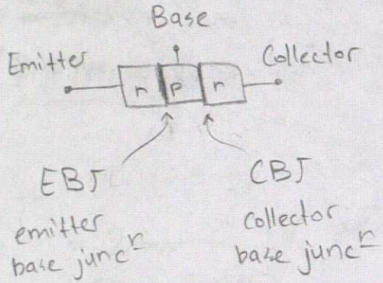


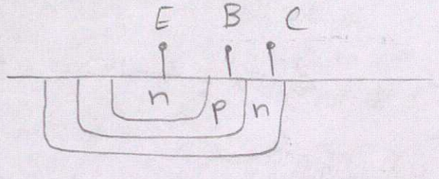
(pnp)



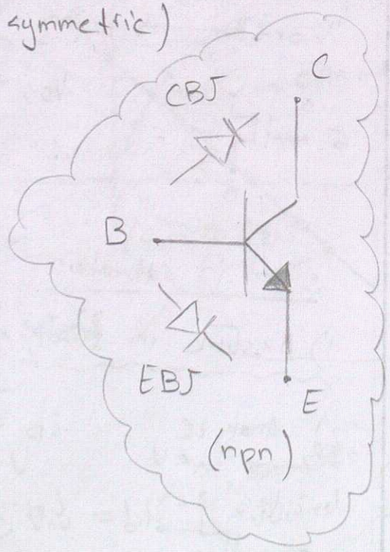
(npn)

Structure





(not symmetric)

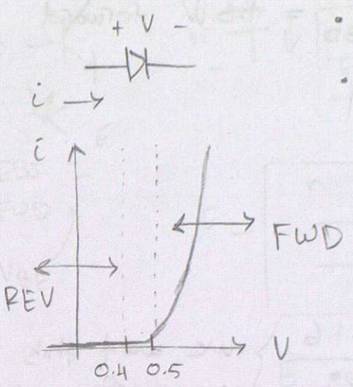


Operating Regions

	EBJ	CBJ
Cutoff	REV	REV
Active	FWD	REV
Saturation	FWD	FWD
reverse-active region	REV	FWD

Mosfet: cutoff, saturation, triode

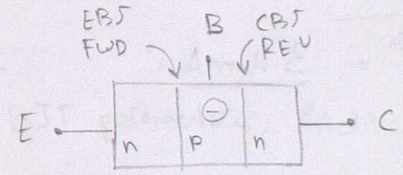
REV vs FWD

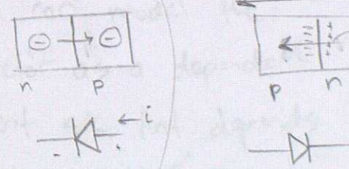


- forward bias when $V > 0.5$ V
- reverse bias when $V < 0.4$ V

- we make base very thin, so electrons "walk a fine line"
- we make collector very thick, so almost all electrons "fall" through

Active Region

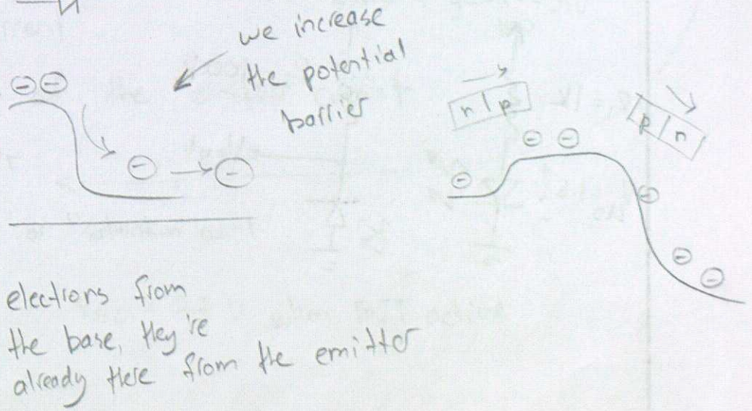




electron flow

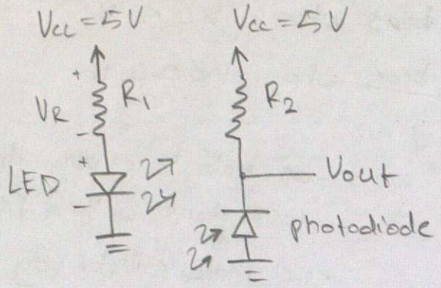
there is a tiny base current

- at the emitter, all the electrons are sent to the base
- at the CBJ, we have a steeper potential barrier, so base electrons will "fall" and end up in the collector



electrons from the base, they're already there from the emitter

Preparation Excersize



$V_{LED} = 1.6\ V$ forward

1) $V = IR \rightarrow I = \frac{V}{R}$

KVL: $V_{LED} + V_R = V_{CC}$

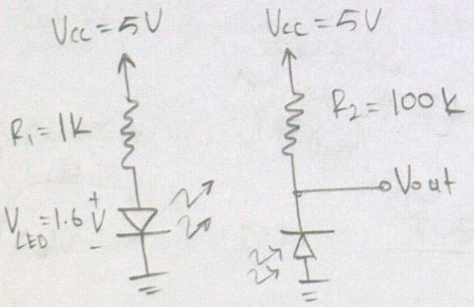
$1.6 + IR_1 = 5$

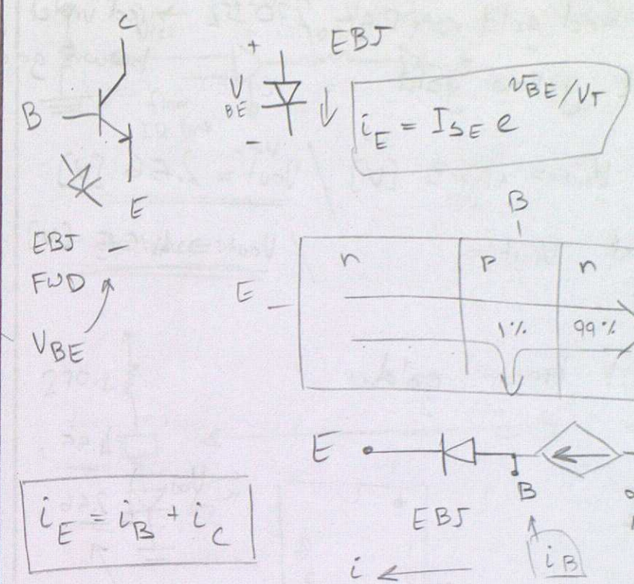
$\rightarrow I = \frac{5-1.6}{R_1}$ } we want this to be a few mA, so we choose R_1 to be some kΩ

Let $R_1 = 1k\Omega \rightarrow I = \frac{5-1.6}{1k} = 3.4\ mA$

2) Let $R_2 = 100\ k\Omega$

Final design





$i_E = i_B + i_C$

BJT parameters: (Active):

$$\alpha = \frac{i_C}{i_E} = \frac{\beta}{\beta+1}$$

$$\beta = \frac{i_C}{i_B} = \frac{\alpha}{1-\alpha}$$

- you can model the collector as a dependent current src that depends on the emitter current
  - ↳ it returns 99% of the emitter current

$i_C = \alpha I_{SE} e^{V_{BE}/V_T}$

I_S ← "scale" or "saturation current"

$i_C = I_S e^{V_{BE}/V_T}$ $\quad V_{BE} \approx 0.7\ V$ when BJT active

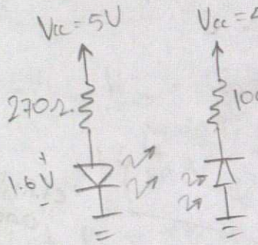
Lab3 Oct 15, 2024

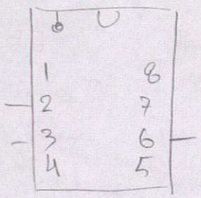
E1) 1k → brown black red gold (pick 270Ω → red violet brown gold)
100k → brown black yellow gold

1) light is passed $V_{out} = 4.23$ [V] / $V_{out} = 2.56$ [V]
2) light is is blocked $V_{out} =$ / $V_{out} = 4.55$ [V]

E2) 100Ω → brown black brown gold

E1)

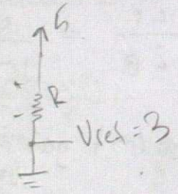




V_{out} { 4.55, 2.56 ↗ $V_{res} = 2.56$

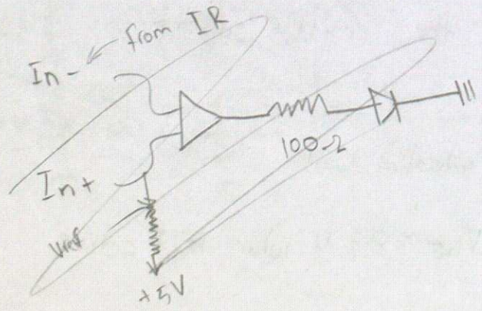
0.1 A ← $V = IR$

10k → brown black orange gold

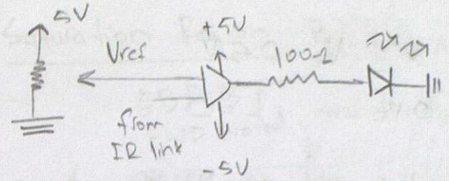


$3 + V_R = 5$
$3 + IR = 5$
$R = \frac{5-3}{I} = \frac{5-3}{0.1} = 20\Omega$

E2)

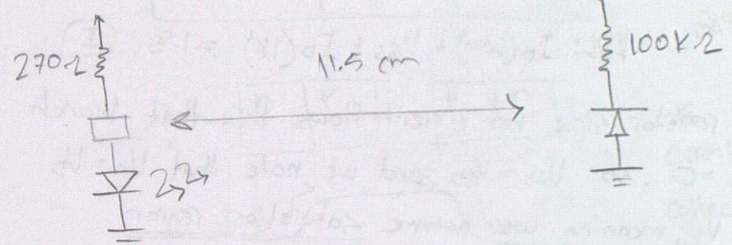


E2)



$V_{ref} = 3V, 4.8V$ (E3)

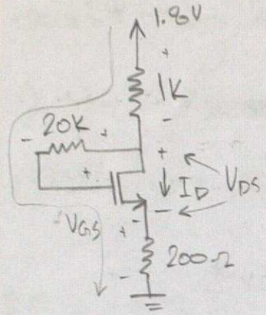
distance:



Problem 1

$\mu_n C_{ox} = 100\,[\mu A/V^2]$ $V_t = 0.5\,V$

$W = 5\,\mu m$, $L = 0.18\,\mu m$, $\lambda = 0$



We note that this is an NMOS and we don't know V_{GS}. We do KVL along left loop to get 2 terms with V_{GS}

KVL: $I_D(200) + V_{GS} + I_D(1K) = 1.8$ (I)

We skip 20k resistor since no current flows thru that branch

We note $V_{DS} = 0$, so $V_{GS} = V_{GD}$, and we note that $V_G = V_D$

so $V_{GD} = 0 < V_t$, meaning we assume saturation region

$$i_D = I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GS} - V_t)^2\,[1 + \lambda V_{DS}]^{\to 0}$$

$$I_D = \frac{1}{2}\left(100\times10^{-6}\right)\left(\frac{5\times10^{-6}}{0.18\times10^{-6}}\right)\left(V_{GS}^2 - 2V_{GS}(0.5) + (0.5)^2\right)$$

$$= \frac{1}{720}\left(V_{GS}^2 - V_{GS} + \frac{1}{4}\right) = \frac{1}{720}V_{GS}^2 - \frac{V_{GS}}{720} + \frac{1}{2880} \quad \text{(II)}$$

(I) $200\,I_D + 1K\,I_D = 1.8 - V_{GS}$

$1200\,I_D = 1.8 - V_{GS}$

$I_D = \frac{3}{2000} - \frac{1}{1200}V_{GS}$

(I) = (II): $\frac{3}{2000} - \frac{1}{1200}V_{GS} = \frac{1}{720}V_{GS}^2 - \frac{V_{GS}}{720} + \frac{1}{2880}$

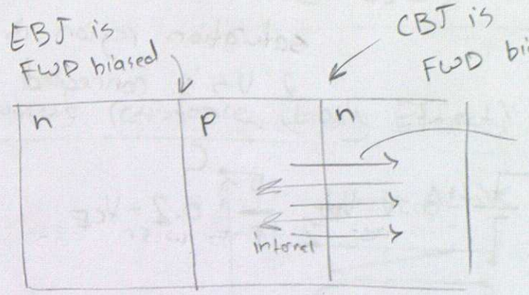
$\frac{1}{720}V_{GS}^2 - \frac{1}{1800}V_{GS} - \frac{83}{72000} = 0$

$\boxed{V_{GS} = 1.133\,V}$ since cut: $V_{GS} = 1.13 > 0.5$, $V_{GD} = 0 < 0.5$

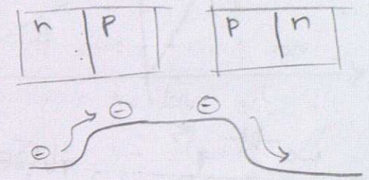
$V_{GS} = -0.733$

$\therefore I_D = 5.56\times10^{-4}\,[A]$

Saturation Region BJT's



this electric field comes from our external voltage that forward biases our CBJ



we still have emitter current that goes to the collector, but it's less than in the active region

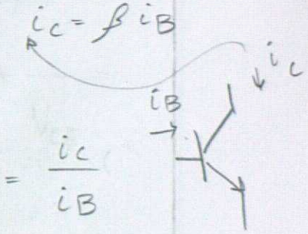
With collector-base junction (CBJ) FWD biased, collector efficiency drops

$\beta = \frac{I_C}{I_B} \approx 100$

$i_E = i_C + i_B$

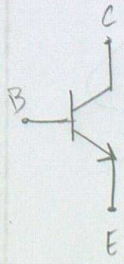
99% 1% in Active Region

$\beta = \frac{i_C}{i_B}$



$i_E = i_C \searrow + i_B \nearrow$

in Saturation Region



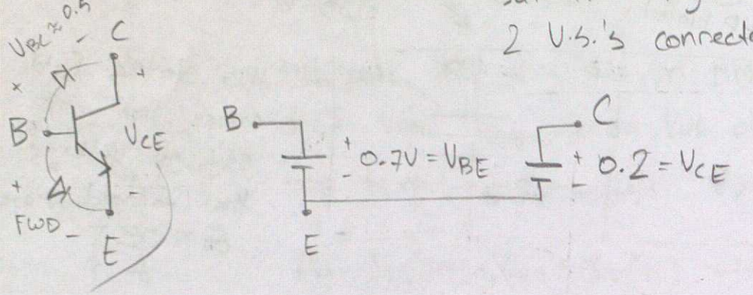
$\beta_{forced} \equiv \frac{I_C \searrow}{I_B \nearrow} < \beta$ ← from active region

$\therefore \beta_{forced} < \beta$

← condition used to verify BJT region

Model in Sat

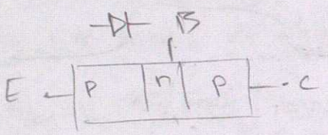
model for BJT in saturation region is like 2 V.S.'s connected



$V_{CE} = 0.7 - 0.5$

$V_{CE} = 0.2$

The pnp BJT

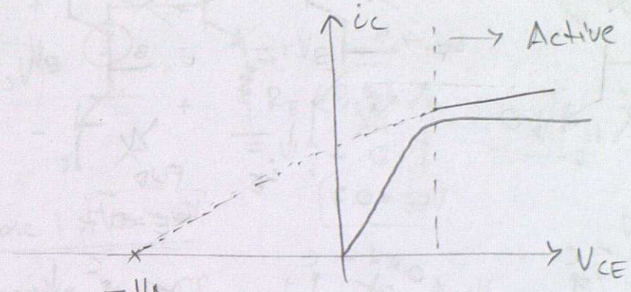


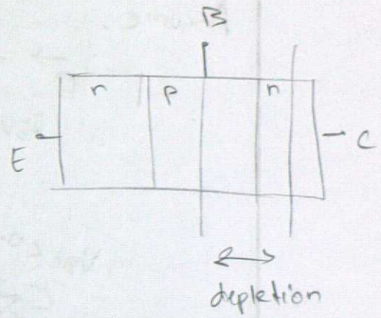
- treat electrons in npn scenario as holes in pnp case

Operation in Active: $\boxed{i_C = I_S e^{V_{BE}/V_T}}$

Finite output resistance (Early Effect)

Early Voltage, V_A [V]





$$i_C = I e^{V_{BE}/V_T} \left[1 + \frac{V_{CE}}{V_A}\right]$$

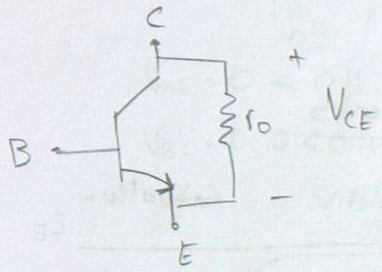
i_C' (without early effect)

$$= i_C' + \underbrace{\frac{i_C'}{V_A}}_{\frac{1}{r_o}} \cdot V_{CE}$$

$$\boxed{r_o = \frac{V_A}{i_C'}}$$

output resistance

Model Early Effect

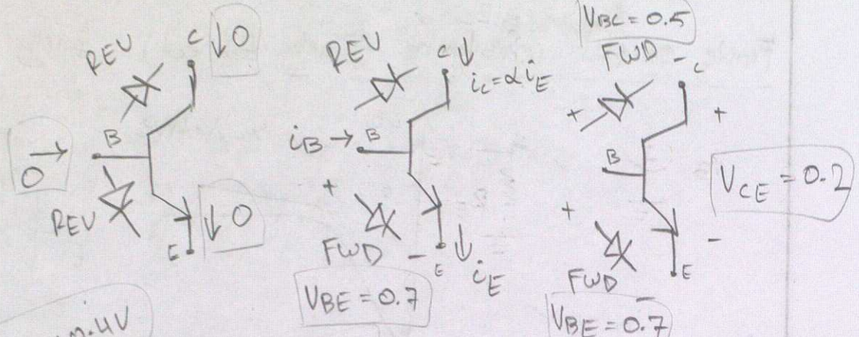


- (Active)
- (no early effect)

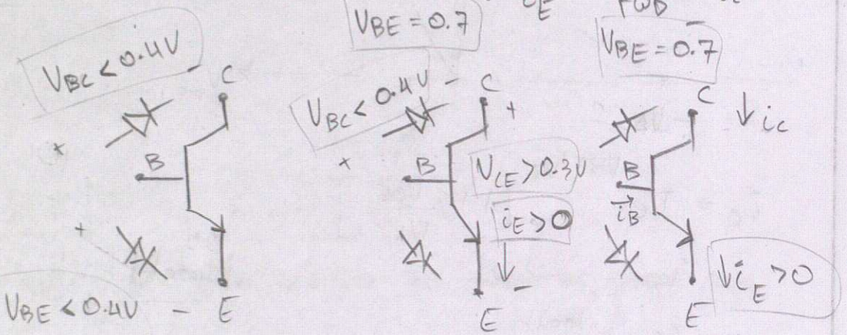
Verifying Operating Regions BJT's (npn)

Cutoff | Active | Saturation

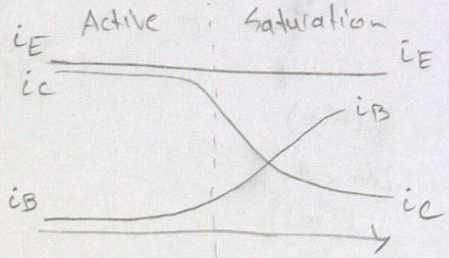
Assume



Verify



Currents



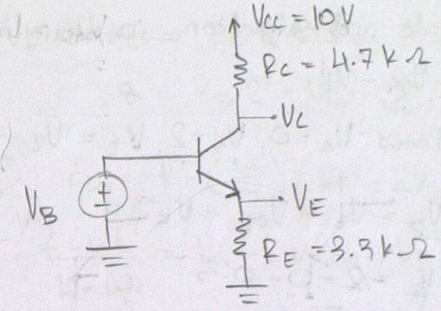
check

$$\beta_{forced} = \frac{i_C}{i_B} < \beta_{Active}$$

(eg. $\beta = 100$)

↑ actual one

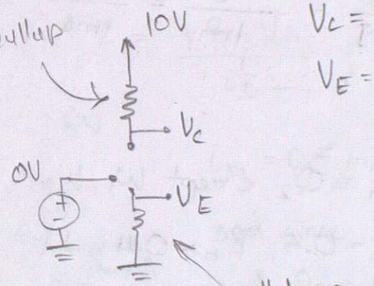
BJT Analysis Example



Case 1: $V_B = 0$

1) assume cutoff

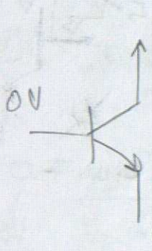
2) pullup



$V_C = 10V$

$V_E = 0V$

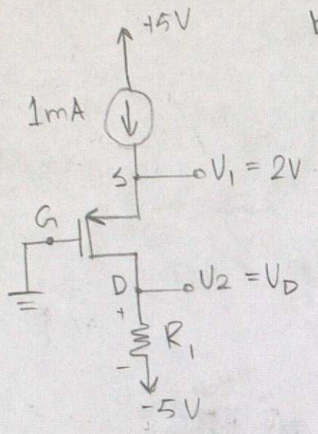
3) Verify



$V_{BE} = 0 < 0.4$ ✓ EBJ Rev

$V_{BC} = 0-10 < 0.4$ ✓ CBJ Rev

Problem 2



$\therefore R_1 = 5.5\ k$ ✓

$|V_t| = 0.5\ V$, design R_1 s.t. PMOS in boundary bet/n triode and saturation. $\therefore V_{SD} = V_{ov}$

$V_{SD} = V_{SG} - |V_t|$

We know $V_G = 0$, $V_S = 2$, $V_D = V_2$

$V_S - V_D = V_S - V_G - V_t$

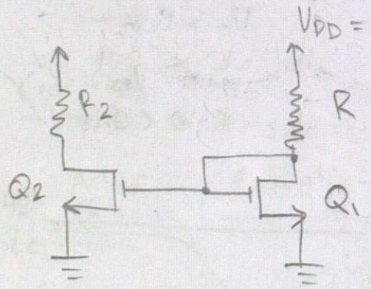
$2 - V_2 = 2 - 0 - 0.5$

$V_2 = 2 - 2 + 0.5 = 0.5 = V_D$

$V = IR$

$R_1 = \frac{V}{I} = \frac{V_2 - (-5)}{1m} = \frac{0.5 + 5}{1mA} = 5.5\ k$

Problem 3



$Q_1 \equiv Q_2$ except W_1, W_2

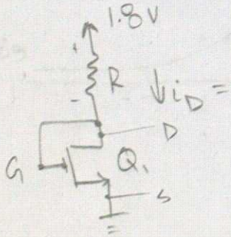
$V_t = 0.5$, $k'_n = 0.4\ mA/V^2$

$L_1 = L_2 = 0.36\ \mu m$, $W_1 = 1.44\ \mu m$

$\lambda = 0$

$R = ?$ for $(Q_1)\ i_D = 50\mu A$

a)



- NMOS, not cutoff
- $V_S = 0 \Rightarrow V_{GD} = 0 < V_t$, so saturation

$i_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GS} - V_t)^2 [1 + \lambda V_{DS}]$ ($\lambda V_{DS} \to 0$)

k'_n ; $V_{GS} - V_t$; $V_G - V_S$, $V_G - 0 = V_G$

MOSFET: $i_D = \frac{1}{2}k'_n\left(\frac{W}{L}\right)(V_G - V_t)^2$ (I)

KVL: $1.8 = i_D R + V_{DS}$

$1.8 = i_D R + V_G$ (II)

$V_D = V_G$

$V_{DS} = V_D - V_S = V_D - 0 = V_D$

✓ $\therefore R_1 = 21\ [k\Omega]$

(I) $i_D = \frac{1}{2}k'_n\left(\frac{W}{L}\right)(V_G^2 - 2V_G V_t + V_t^2)$

$\frac{2 i_D L}{k'_n W} = V_G^2 - 2V_G V_t + V_t^2$

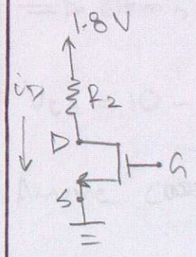
$0 = V_G^2 - 2V_t V_G + V_t^2 - \frac{2 i_D L}{k'_n W}$

this would put us in cutoff ↓

$0 = V_G^2 - V_G + \frac{3}{16} \longrightarrow V_G = 0.75$, $V_G = 0.25$

(II) $R = \frac{1.8 - V_G}{i_D} = \frac{1.8 - 0.75\ [V]}{50\mu A} = 21000 \approx 21\ [k\Omega]$

b)



$i_D = 0.5\ mA$, $V_{GD} = V_t = 0.5$ or $V_{DS} = V_{GS} - V_t$

and since $V_S = 0$, we have: $V_D = V_G - V_t$

and from part a) $V_G = 0.75 \Rightarrow V_D = 0.75 - 0.5$

$V_D = 0.25\ [V]$

KVL: $1.8 = R_2 i_D + V_{DS}$

$R_2 = \frac{1.8 - V_D - V_S}{i_D} = \frac{1.8 - 0.25}{0.5\ mA} = 3.1\ [k\Omega]$

choose saturation eqn (V_G)

$i_D = \frac{1}{2}k'_n \frac{W_2}{L_2}(V_{GS} - V_t)^2$

$W_2 = \frac{2 L_2 i_D}{k'_n (V_G - V_t)^2} = 1.44 \times 10^{-5}\ m$

$= 14.4 \times 10^{-6}\ m$

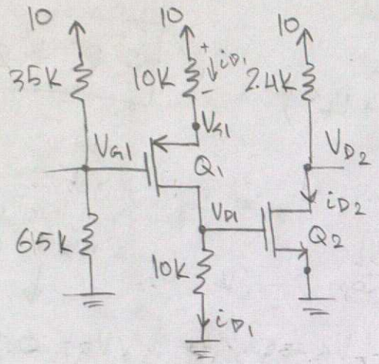
✓ $\therefore R_2 = 3.1\ k\Omega$

$W_2 = 14.4\ \mu m$

Tutorial 6 (MOSFET DC) Oct 20, 2024

Problem 1

a) Assume no channel length modulation



1) Voltage division $\Rightarrow V_{G1}$

$$V_{G1} = 10\left(\frac{65k}{35k+65k}\right) = \underline{6.5\,V = V_{G1}}$$

2) Q_1 is PMOS, assume saturation

$$i_{D1} = \frac{1}{2}\mu_p C_{ox}\frac{W}{L}(V_{SG} - V_t)^2 \quad (I)$$

↳ KVL: $V_{G1} + V_{SG} + 10K(i_{D1}) = 10$

(I) $i_{D1} = \frac{1}{2}(0.1\times10^{-3})\left(\frac{20}{0.5}\right)(V_{SG}^2 - 2V_tV_{SG} + V_t^2)$

$$i_{D1} = \frac{1}{500}V_{SG}^2 - \frac{2(1.2)}{500}V_{SG} + \frac{(1.2)^2}{500}$$

(II) $V_{G1} + V_{SG} + 10K\,i_{D1} = 10$

$$i_{D1} = \frac{10 - V_{G1} - V_{SG}}{10k} = \frac{10}{10k} - \frac{6.5}{10k} - \frac{1}{10k}V_{SG}$$

(I)=(II) $\frac{1}{1000} - \frac{13}{20000} - \frac{1}{10k}V_{SG} = \frac{1}{500}V_{SG}^2 - \frac{3}{625}V_{SG} + \frac{9}{3125}$

$$0 = \frac{1}{500}V_{SG}^2 - \frac{47}{10000}V_{SG} + \frac{253}{100000}$$

$\underline{V_{SG} = 1.51503\,V}$, $V_{SG} = 0.834$ ← puts us in cutoff

$V_{SG} = V_S - V_G$

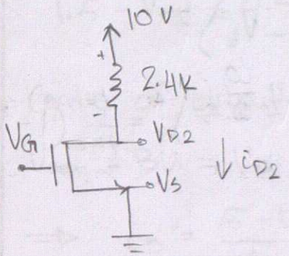
$V_S = V_{SG} + V_G = 1.515 + 6.5 = \underline{8.015\,V = V_S}$

$$i_D = \frac{10}{10k} - \frac{6.5}{10k} - \frac{1}{10k}(1.51503) = 1.98\times10^{-4}\,A = \underline{0.198\,mA}$$

$\therefore V_{S1} = 8.015\,V$, $V_{G1} = 6.5\,V$, $i_{D1} = 0.198\,mA$ ✓ | $\therefore V_{D1} = 1.98\,V$ ✓

$V_{D1} = 10k\,i_{D1} = 10K(1.98\times10^{-4}) = 1.98\,V$

3) Q_2 NMOS, assume saturation



$V_{G2} = V_{D1} = 1.98\,V$, $V_S = 0 \rightarrow V_{GS} = 1.98\,V$

$$i_{D2} = \frac{1}{2}(\mu_n C_{ox})\frac{W}{L}(V_{GS} - V_t)^2$$

$$= \frac{1}{2}(0.25\times10^{-3})\left(\frac{10}{0.5}\right)(1.98 - 1)^2$$

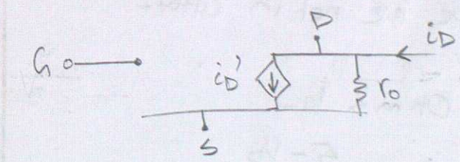
$$= 2.401\times10^{-3} = 2.4\,mA$$

⇒ Ohm's law: $i_{D2} = \frac{10 - V_{D2}}{2.4K}$

$V_{D2} = 10 - 2.4K(2.4mA) = 4.24\,V$

$\therefore i_{D2} = 2.4\,mA$ ✓
$V_{D2} = 4.24\,V$ ✓

b) Assume CWM for Q_2:



$$i_D = i_D' + \frac{V_{DS}}{r_o}$$

$$r_o = \frac{1}{i_D'\lambda} = \frac{1}{(2.4\,mA)(0.02)}$$

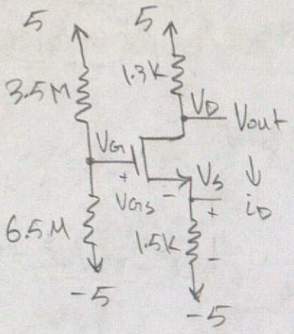
$r_o = 20833\,\Omega = 20.8\,k\Omega$

$\therefore i_D = (2.4mA) + \frac{V_{DS}}{20.8k}$ (I)

(II) $i_D = \frac{10 - V_D}{2.4K}$

Problem 2

a)



1) KCL: $\frac{5-V_G}{3.5M} - \frac{V_G-(-5)}{6.5M} \Rightarrow \frac{5}{3.5M} - \frac{V_G}{3.5M} = \frac{V_G}{6.5M} + \frac{5}{6.5M}$

$-\frac{V_G}{3.5M} - \frac{V_G}{6.5M} = \frac{5}{6.5M} - \frac{5}{3.5M} \Rightarrow V_G = \frac{5/6.5M - 5/3.5M}{-\frac{1}{3.5M} - \frac{1}{6.5M}}$

2) Assume saturation (NMOS), $V_G = 1.5$ V

$i_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GS}-V_t)^2$

$i_D = \frac{1}{750}(V_G - V_S - V_t)^2$

$i_D = \frac{1}{750}(1.5 - V_S - 0.5)^2 = \frac{1}{750}(1-V_S)^2$

$i_D = \frac{1}{750}(1^2 - 2(1)V_S + V_S^2)$

3) do Ohm's law: $i_D = \frac{V_S-(-5)}{1.5K} = \frac{-0.5+5}{1.5K} = 3mA$

4) equate 2) and 3) $\frac{V_S+5}{1.5K} = \frac{1}{750}(1 - 2V_S + V_S^2)$

$V_S + 5 = 2(1 - 2V_S + V_S^2)$

$V_S + 5 = 2 - 4V_S + 2V_S^2$

$0 = 2V_S^2 - 5V_S - 3$

$V_S = 3 \quad V_S = -0.5$

4) You pick $V_S = -0.5$ so we are not in cutoff.

$V_{GS_1} = 1.5 - 3 = -1.5$

$V_{GS_2} = 1.5 - (-0.5) = 2$

5) Ohm's law

$i_D = \frac{5-V_D}{1.3K}$

$V_D = 5 - 1.3K(3mA) = 1.1\,V = V_D$

$V_{GD} = 1.5 - 1.1 = 0.4 < V_t$

∴ Yes saturation, $V_G = 1.5$ V, $V_S = -0.5$ V, $V_D = 1.1$ V

b) We know by default our absolute bounds for Vout are the V_{DD} and $-V_{SS}$ $\Rightarrow -5 \le V_{out} \le 5$ (I)

Then we find range to keep MOSFET in saturation

$V_{GD} \le V_t$

$V_G - V_D \le 0.5$

$1.5 - V_{out} \le 0.5$

$\Rightarrow 1.5 - 0.5 \le V_{out}$

$\therefore V_{out} \ge 1$ V (II)

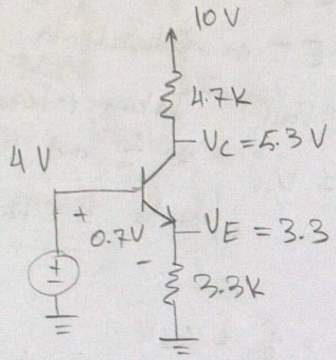
Taking intersection of (I) and (II) we get: $1 \le V_{out} \le 5$

c) Centre of output voltage is $\frac{5+1}{2} = \frac{6}{2} = 3$V

$V_{out} = 3V = V_D$

$\Rightarrow i_D = \frac{5-V_D}{R_D} \Rightarrow R_D = \frac{5-3}{3mA} = 666.67\,\Omega = R_D$

Case 2: $V_B = 4V$



1) Assume ACTIVE

2). You know V_E is 0.7 lower than V_B

$\cdot i_E = \frac{3.3-0}{3.3k} = 1\,mA$

$\cdot i_C = \alpha I_E = (0.99)(1mA) = 0.99\,mA$

$\beta = 100$

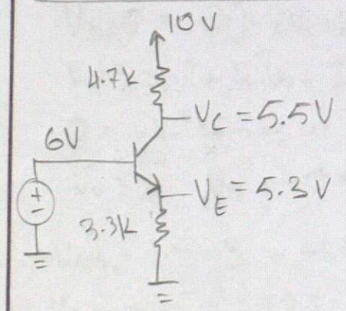
$\alpha = \frac{\beta}{\beta+1} = \frac{100}{101} = 0.99$

$\cdot i_C = \frac{10 - V_C}{4.7k}$

$(0.99mA)(4.7k) = 10 - V_C \Longrightarrow V_C = 10 - (0.99 \times 4.7) = 5.3V$

3) Verify that $V_{CE} > 0.3 \Longrightarrow 5.3 - 3.3 = 2 > 0.3$ ✓

Case 3: $V_B = 6V$



1) Assume Saturation

2) $V_{BE} = 0.7$, $V_{EC} = 0.2$

$i_E = \frac{5.3-0}{3.3k} = 1.6\,mA$

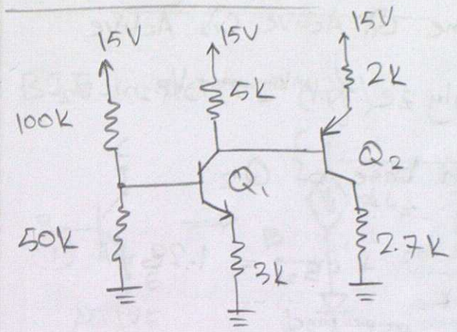
$i_C = \frac{10-5.5}{4.7k} = 0.96\,mA$

$i_E = i_B + i_C \Longrightarrow i_B = 0.64\,mA$

3) Verify $\beta_{forced} < \beta_{active}$

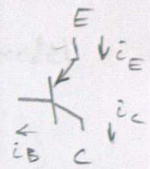
$\beta_{forced} = \frac{i_C}{i_B} = \frac{0.96}{0.64} = 1.5 < 100$ ✓

Ex 2: npn + pnp

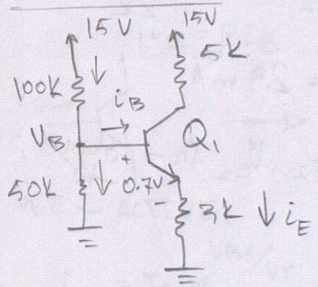


$\beta = 100$ for both

pnp



Focus on Q_1



1) Assume Q_1 in Active (and Q_2)

2) ① KCL: $\frac{15 - V_B}{100k} = i_B + \frac{V_B - 0}{50k}$

$\frac{15 - V_B}{100k} \overset{?}{=} \frac{V_B}{50k} + i_B \overset{?}{\ldots}$

② $i_E = \frac{V_B - 0.7}{3k} \quad \therefore i_B = \frac{i_E}{\beta+1}$

$\frac{15 - V_B}{100k} = \frac{V_B}{50k} + \frac{1}{\beta+1} \times \frac{V_B - 0.7}{3k}$

$\begin{cases} V_B = 4.57 \\ i_E = i_C + i_B \\ 1.29 = 1.28 + 0.01 \ [mA] \end{cases}$

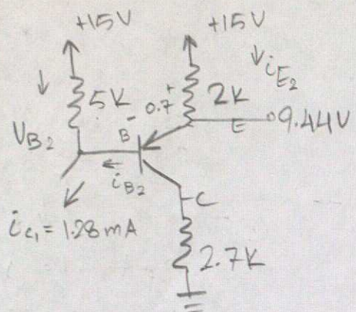
$i_E = i_C + i_B$

$= \beta i_B + i_B$

$= (\beta+1) i_B$

Week 8: Lecture 2 — Oct 23, 2024

Focus on Q_2



1) Assume Q_1 Active, Q_2 Active

2) Analyze { unknowns: V_{B_2}, i_{B_2}

KCL @ base of Q_2

$$\frac{15 - V_{B_2}}{5K} + i_{B_2} = 1.28\,mA \quad (I)$$

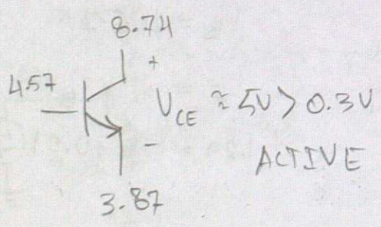
but $i_{E_2} = \frac{15 - (V_{B_2}+0.7)}{2K}$ $\Rightarrow$ $(\beta+1) i_{B_2} = \frac{15-(V_{B_2}+0.7)}{2K}$ (II) (see prev page)

Using (I) and (II): $V_{B_2} = 8.74V$, $i_{E_2} = 2.9\,mA$

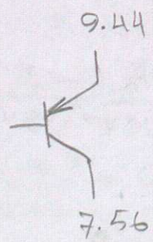
$i_{C_2} = \alpha i_{E_2} = 2.8\,mA$ find $i_{C_2}, V_{E_2}, V_{C_2}$ from above

Verify

Q_1

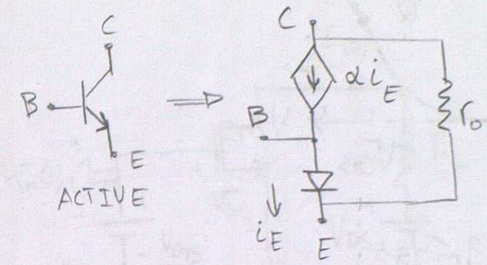


Q_2



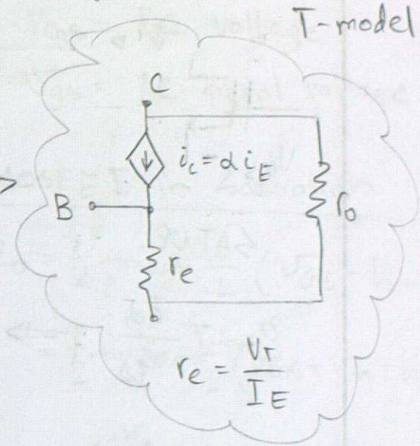
Small Signal Transistors

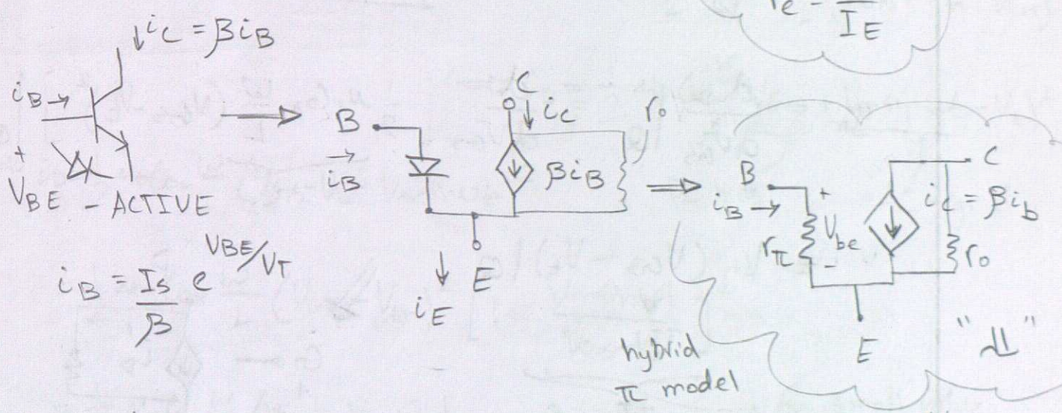
BJT in ACTIVE (npn)



(focused on i_E)

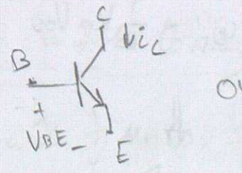
T-model



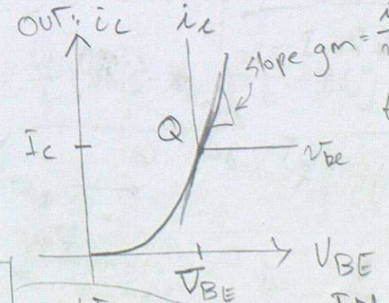


$r_\pi = \frac{V_T}{i_B} = (\beta+1) r_e$

Parameters



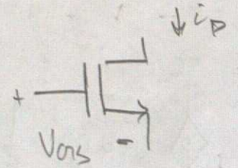
Input is V_{BE}, output is i_C



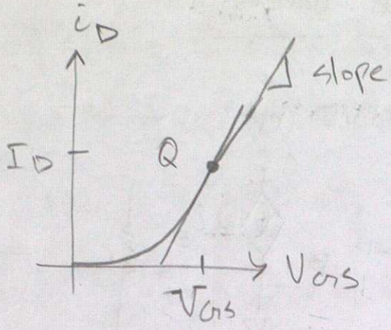
$$g_m = \frac{I_C}{V_T} = \frac{\alpha I_E}{V_T} = \alpha / r_e$$

$$g_m = \frac{di_c}{dV_{BE}}\Big|_{Q=(I_C, V_{BE})}$$

MOSFET



SATUR.



$$g_m = \frac{i_d}{v_{gs}} \Rightarrow i_d = g_m v_{gs}$$

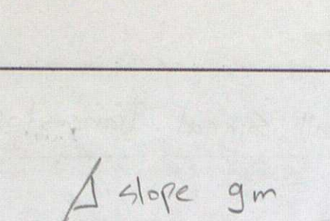
$$g_m = \frac{di_D}{dv_{GS}}\Big|_Q = \frac{d}{dv_{GS}}\left[\underbrace{\frac{1}{2}\mu_n C_{ox}\frac{W}{L}}_{K_n}(V_{GS}-V_t)^2\right]\Big|_Q$$

$$= k_n (V_{GS}-V_t)\Big|_Q$$

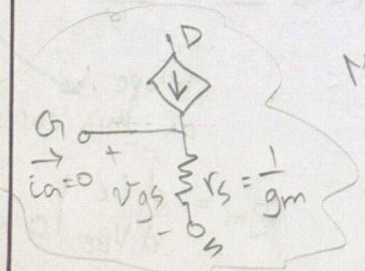
V_{GS} → V_{ov}

$$= k_n V_{ov}$$

$$\boxed{g_m = k_n V_{ov} = \sqrt{2 k_n I_D}}$$

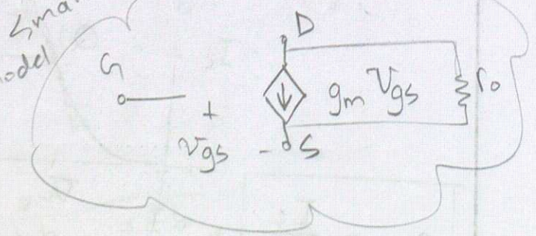


$$i_D' = \frac{1}{2} k_n V_{ov}^2$$



π-model

MOSFET small signal T-model



Transistor Small Signal Models (Wang Notes)

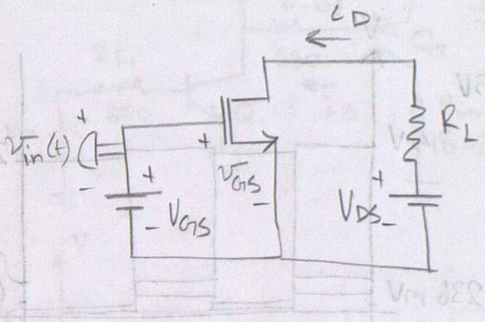
Large Signal Operation

v_{GS} = total voltage

V_{GS} = DC voltage

v_{gs} = AC signal voltage

$v_{in}(t) = V_m \sin\omega t$



MOSFET in Saturation

$$i_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(v_{GS}-V_{tn})^2$$

$$= \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}+v_{in}-V_{tn})^2$$

$$\Rightarrow i_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(\underbrace{V_{GS}}_{\text{DC bias}} + \underbrace{V_m\sin\omega t}_{\text{AC signal}} - V_t)^2$$

$$\Rightarrow i_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_t+V_m\sin\omega t)^2$$

$$= \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{tn})^2\left[1+\frac{V_m\sin\omega t}{V_{GS}-V_{tn}}\right]^2$$

$$= \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{tn})^2[1+\zeta]^2$$

ζ: small value ($\zeta \ll 1$)

$$\frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{tn})^2[1+2\zeta+\zeta^2]$$

drop the ζ^2 term

$$\simeq \underbrace{\frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{tn})^2}_{I_D}[1+2\zeta]$$

$$\simeq I_D\left[1+2\frac{V_m\sin\omega t}{V_{GS}-V_{tn}}\right]$$

$$\boxed{i_D \simeq I_D + \frac{2I_D}{V_{GS}-V_{tn}}V_m\sin\omega t}$$

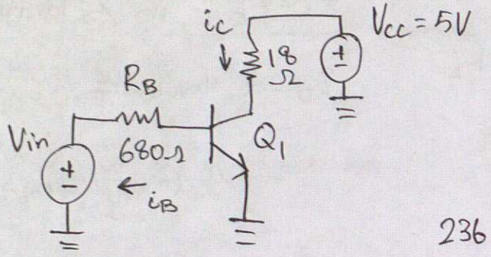
small signal

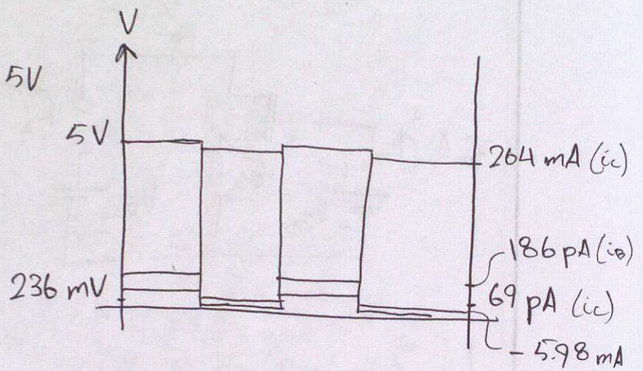
total — DC bias — transconductance g_m

Lab 4 Prelab — Nov 2, 2024

1.a) $f = 100\,Hz \Rightarrow T = 0.01\,s$ = period

Duty Cycle = $\frac{T_{on}}{period} \Rightarrow T_{on} = (50\%)(0.01s) = 5\,ms$





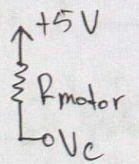
b) When BJT is on, $V_{collector} \simeq 0$

$\Rightarrow i_C \approx 264\,mA$ $\quad \beta_{forced} = \frac{i_C}{i_B} = \frac{264\,mA}{5.98\,mA} = 44.15$

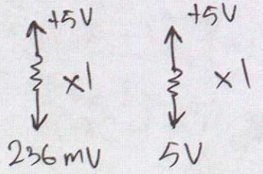
$\Rightarrow i_B \approx -5.98\,mA$

$\beta_{active} = 50$, so since $\beta_{forced} = 44.15 < \beta_{active} = 50$ $\quad$ ∴ Saturation

c)



V_c varies from 236 mV to 5V



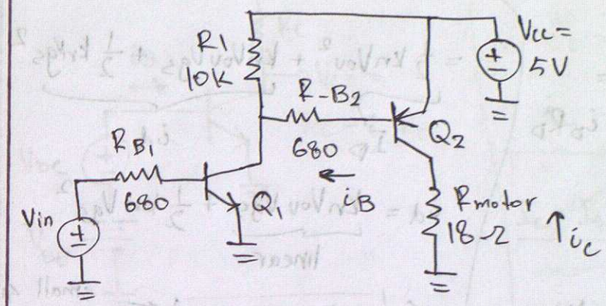
$V_{av_1} = \frac{[5 - 236mV] + [5 - 5]}{2}$

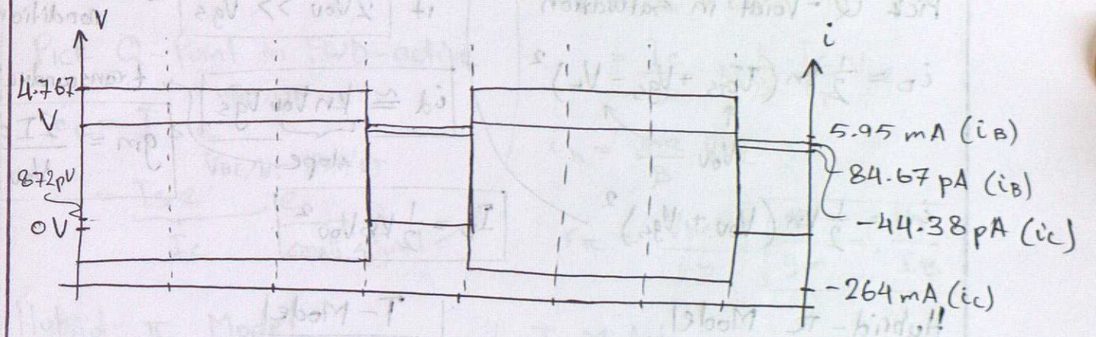
$V_{av} = 2.382\,V$

Since $V_{av} = 2.38\,V$, motor speed ≈ ~~1000~~ 900 rpm

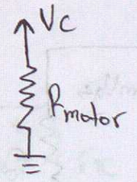
2.a) $T_{on} = (75\%)(0.01s) = 7.5\,ms = 0.0075s$

When Q_2 is ON
↳ $i_B = 5.95\,mA$
↳ $i_C = -264\,mA$

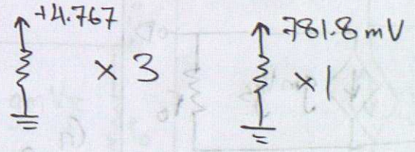




b)



V_c varies from 4.767 V to 781.8 mV

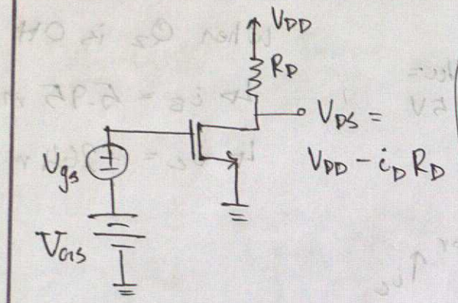


∴ $V_{av} = \frac{3(4.767) + 1(781.8mV)}{4} = 3.771\,V$

Since $V_{av} = 3.77\,V$, motor speed ≈ 1500 rpm

Transistor Small Signal Models

The MOSFET Case



Pick Q-Point in Saturation

$$i_D = \frac{1}{2} k_n (V_{GS} + V_{gs} - V_t)^2$$

$V_{GS} \rightarrow V_{ov}$

$$i_D = \frac{1}{2} k_n (V_{ov} + V_{gs})^2$$

$$i_D = \frac{1}{2} k_n (V_{ov}^2 + 2 V_{ov} V_{gs} + V_{gs}^2)$$

$$= \underbrace{\frac{1}{2} k_n V_{ov}^2}_{I_D} + \underbrace{k_n V_{ov} V_{gs} + \frac{1}{2} k_n V_{gs}^2}_{i_d}$$

$$i_d = \underbrace{k_n V_{ov} V_{gs}}_{\text{linear}} + \frac{1}{2} k_n V_{gs}^2$$

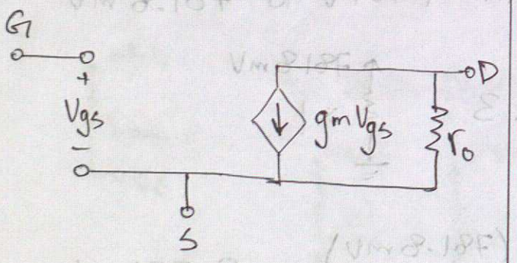
if $\boxed{2V_{ov} >> V_{gs}}$ ← small signal condition

$$\boxed{i_d \cong k_n V_{ov} V_{gs}}$$ slope → transconductance

$$\boxed{g_m = \frac{2 I_D}{V_{ov}}}$$

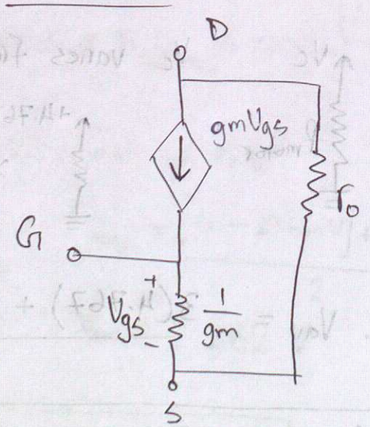
$$\boxed{I_D = \frac{1}{2} k_n V_{ov}^2}$$

Hybrid-π Model

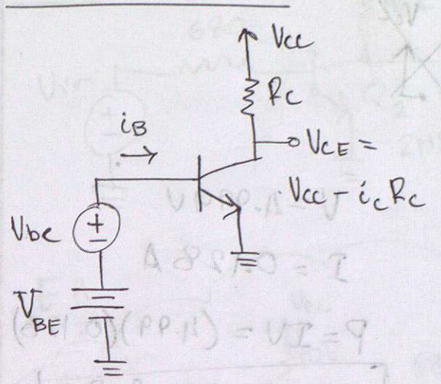


$$r_o = \frac{|V_A|}{I_D} \qquad V_A = \frac{1}{\lambda}$$

T-Model



The BJT Case



Pick Q-Point in FWD-active

$$i_C = I_S e^{V_{BE}/V_T}$$

$$= \underbrace{I_S e^{V_{BE}/V_T}}_{I_C} \underbrace{e^{v_{be}/V_T}}_{\text{small signal}}$$

$$e^{\frac{V_{be}}{V_T}} \approx 1 + \frac{V_{be}}{V_T} \quad \text{if } \boxed{V_T >> V_{be}}$$ ← small signal condition

$$\therefore i_C = I_C \left(1 + \frac{V_{be}}{V_T}\right)$$

$$i_C = I_C + \frac{I_C}{V_T} V_{be}$$

$\boxed{I_C = I_S e^{\frac{V_{BE}}{V_T}}}$ slope → $\boxed{g_m = \frac{I_C}{V_T}}$

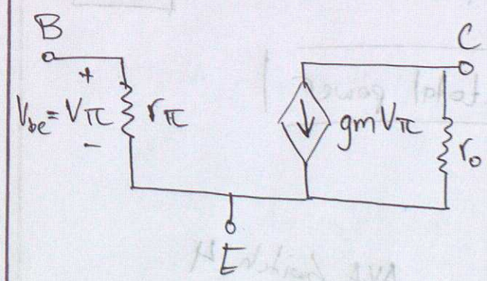
$$i_B = I_B + i_b$$

$$= \frac{I_C}{\beta} + \frac{1}{\beta} \frac{I_C}{V_T} V_{be}$$

$$i_b = \frac{g_m}{\beta} V_{be}$$

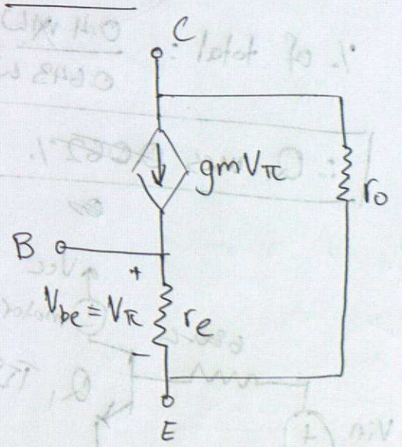
$$r_\pi = \frac{V_{be}}{i_b} = \boxed{\frac{\beta}{g_m} = \frac{V_T}{I_B}}$$

Hybrid-π Model



$$r_\pi = \frac{\beta}{g_m} = \frac{V_T}{I_B} \qquad r_o = \frac{|V_A|}{I_C}$$

T-Model

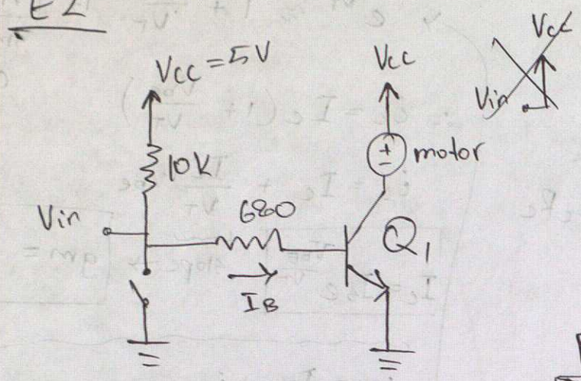


$$r_e = \frac{\alpha}{g_m} = \frac{V_T}{I_E}$$

Lab 4

E2

a)



$V_{in} = 0.945$ [V]

$I_B = 0.432$ mA

$P = (0.945\ V)(0.432\ mA) = 0.4$ mW

$\boxed{P = 0.4\ [\cancel{m}W]}$ (power of Q_1

% of total : $\frac{0.4\ \cancel{m}W}{0.643\ W} \times 100 = \cancel{0.0622}\ \%$ $\boxed{62\ \%}$

$\therefore Q_1$ uses ~~0.062~~ % of total power

$V = 4.999$ V

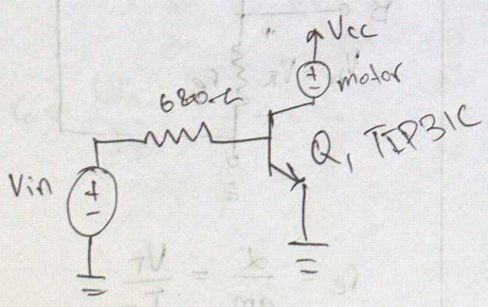
$I = 0.128$ A

$P = IV = (4.99)(0.128)$

$\boxed{P = 0.643\ [W]}$

power of ckt

b)

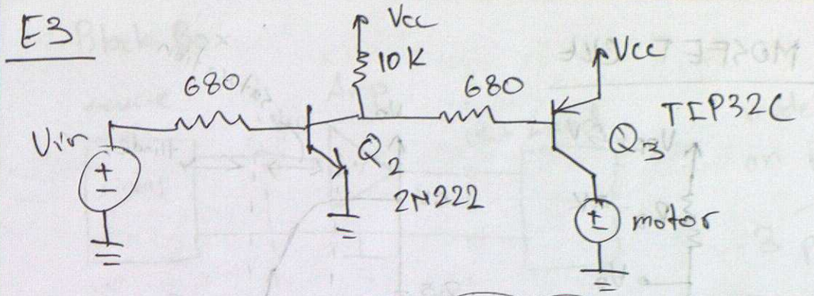


AKA Switch 4

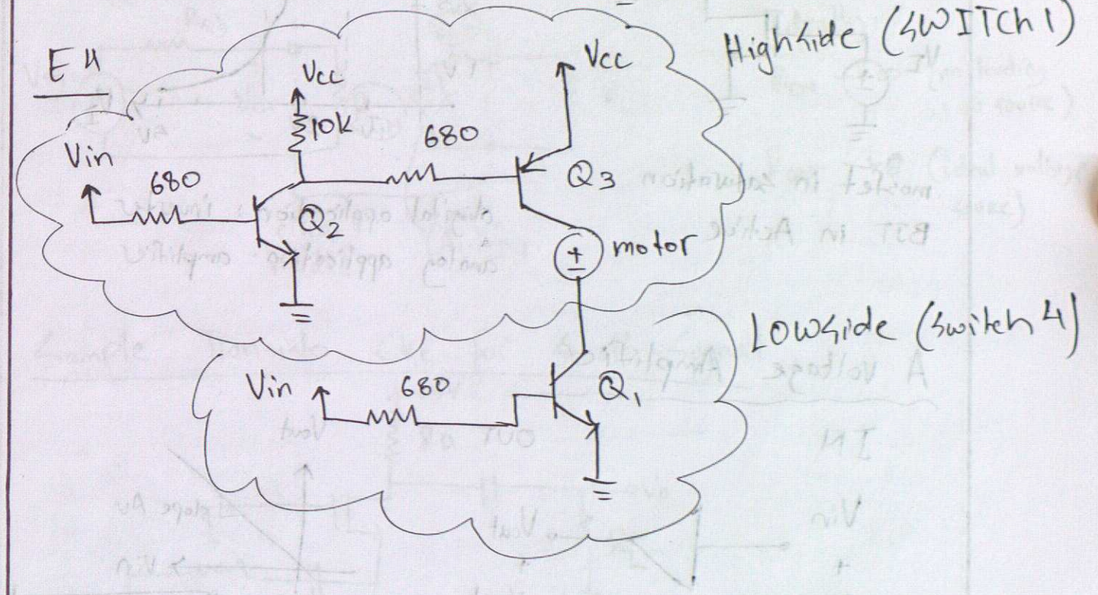
E3

AKA Switch 1

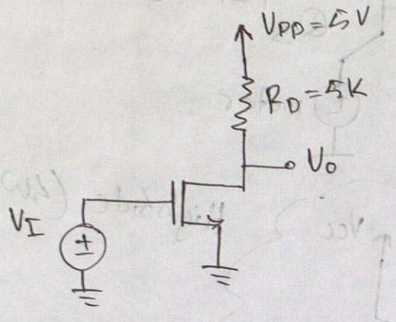
a)

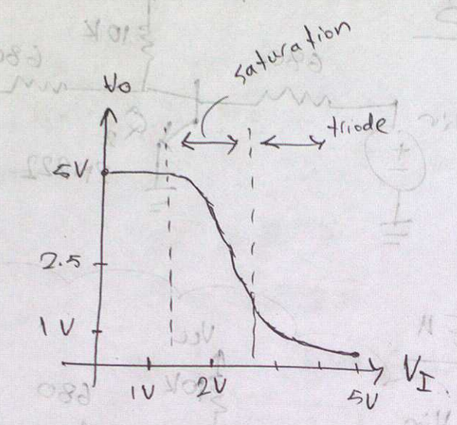


E4



Recall MOSFET CKT

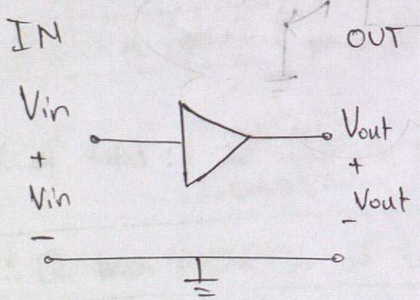


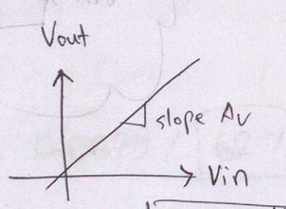


mosfet in saturation
BJT in Active

digital application: inverter
analog application: amplifier

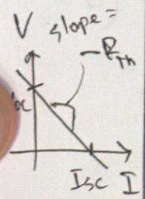
A voltage Amplifier



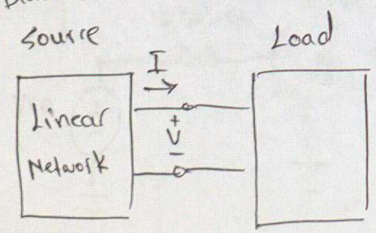


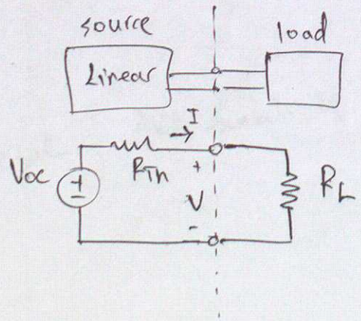
Voltage gain $A_V \equiv \frac{V_{out}}{V_{in}}$

Recall Thevenin

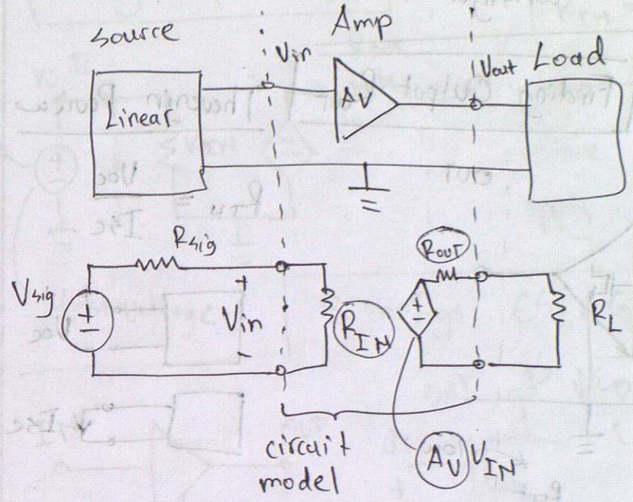


Black Box





Black Box



model ckt based on R_{IN}, R_{OUT}, A_{V_0}

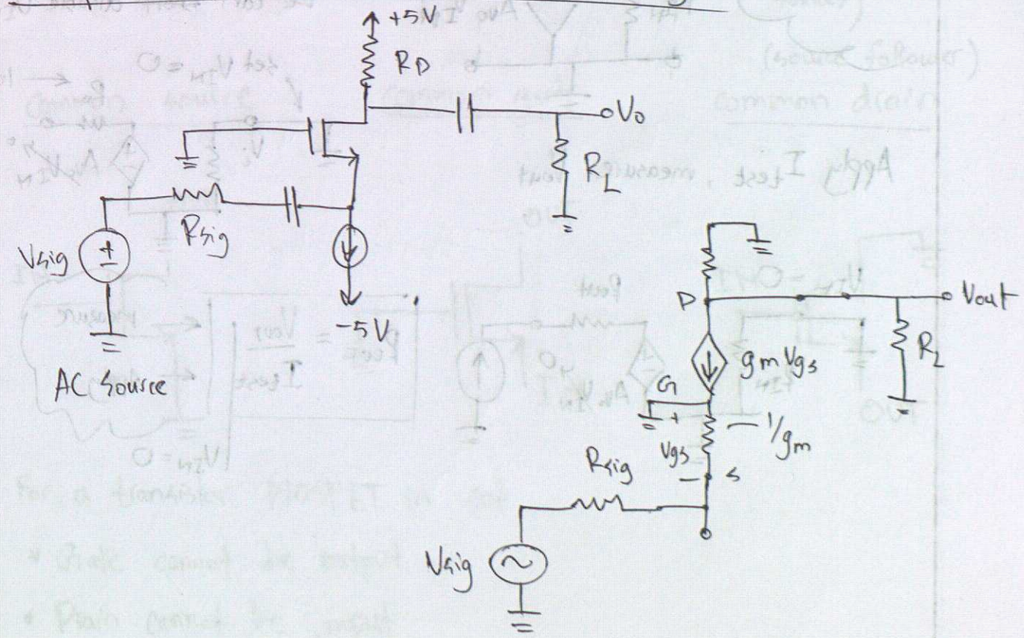
3 parameters

Ideally:

$R_{IN} \to \infty$ (no loading of source)

$R_{OUT} \to 0$ (ideal voltage source)

Sample Transisto CKT for Small Signal



Week 9: Lecture 2

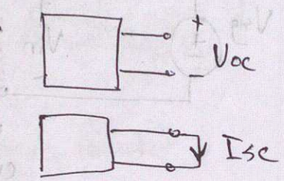
Nov 6, 2024

Transistor Amplifier Configurations

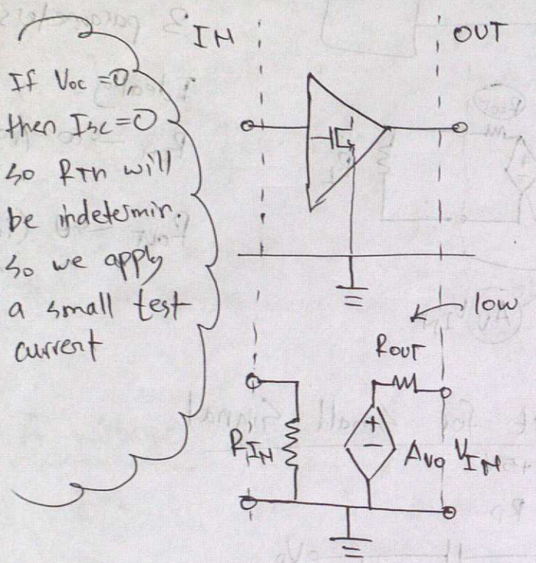
Basic Concept: **Finding Output R_{OUT}**

Thevenin Review

$$R_{TH} = \frac{V_{OC}}{I_{SC}}$$

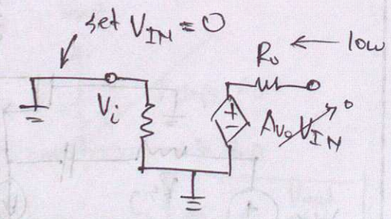


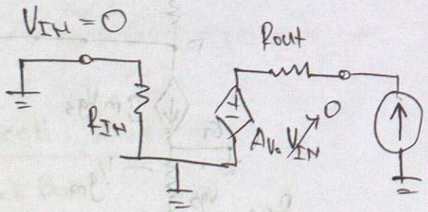
If $V_{OC}=0$, then $I_{SC}=0$ so R_{TH} will be indetermin. so we apply a small test current



Apply I_{test}, measure V_{out}

to easily see R_{OUT}, we can ~~short~~ disable V_{IN}

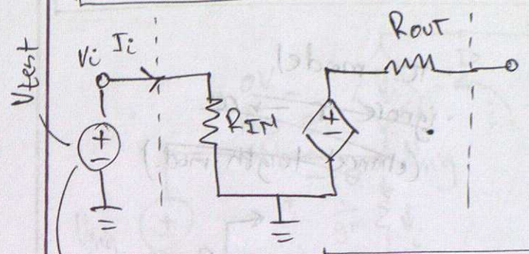




$$R_{OUT} = \frac{V_{OUT}}{I_{test}}$$ ← measure, ← Apply

$V_{IN}=0$

Finding Input R_{IN}



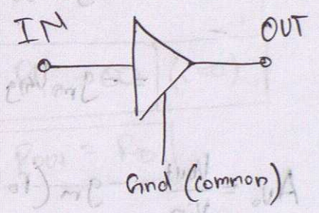
$$R_{IN} = \frac{V_{test}}{I_i}$$ ← Apply, ← measure

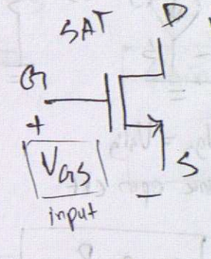
Since R_{IN} large, can apply test voltage V_{test}

Gate can not be output

Drain can not be input

3 configs: CS, CG, CD

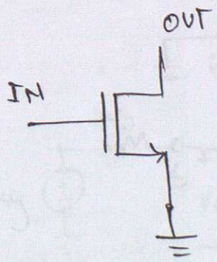




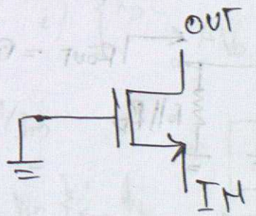
$i_D = f(V_{GS})$ ← output

these "common" grounds are small signal grounds (meaning at DC it's like connected to DC sources)

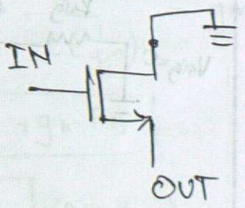
Common source



Common gate



Common drain (source follower)



For a transistor MOSFET in sat

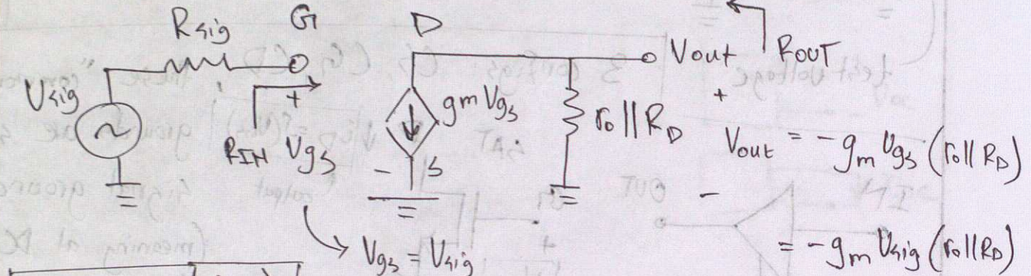
- Gate cannot be output
- Drain cannot be input

Amplifier Charactistics

Gain: $A = \frac{V_o}{V_i}$

Common Source Amp:

- T-model
- ~~ignore $r_o \to \infty$~~ (~~channel length mod.~~)



$V_{out} = -g_m V_{gs} (r_o \| R_D)$

$= -g_m V_{sig} (r_o \| R_D)$

$V_{gs} = V_{sig}$ since open ckt

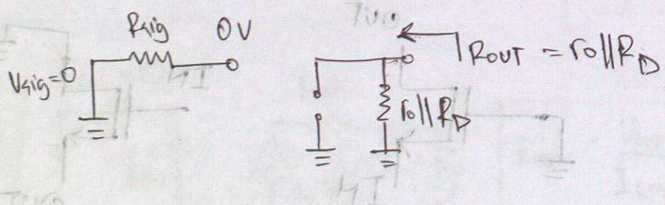
$A_{V_o} = \frac{V_{out}}{V_{in}} = -g_m (r_o \| R_D)$

$R_{in} = \infty$	$(i=0)$

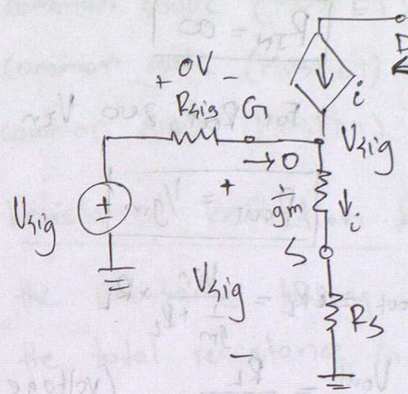
Gain $= -g_m (r_o \| R_D)$	$\approx -g_m R_D$

finding R_{out}: set $V_{sig} = 0$

$R_{out} = r_o \| R_D$	$\approx R_D$



Common Source Amp w/r R_S | T-model, ignore r_o



$V_{sig} = i \times \left(\frac{1}{g_m} + R_S\right)$

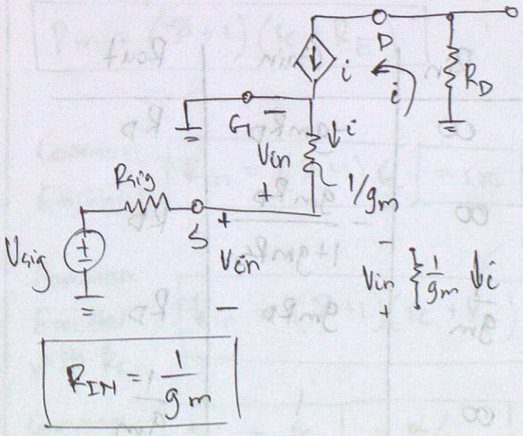
$A_{V_o} = \frac{V_{out}}{V_{in}} = \frac{-iR_D}{i\left(\frac{1}{g_m} + R_S\right)} = -\frac{R_D g_m}{1 + g_m R_D}$

$R_{in} = \infty$	$(i=0)$

$R_{out} = R_D$

Gain $= \frac{-g_m R_D}{1 + g_m R_S}$

Common Gate Amp | T-model, ignore r_o



$A_{V_o} = \frac{V_{out}}{V_{in}} = \frac{-iR_D}{-i\left(\frac{1}{g_m}\right)} = g_m R_D$

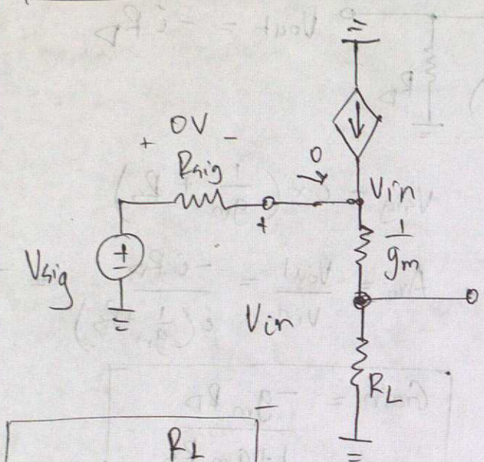
Gain $= +g_m R_D$

$R_{IN} = \frac{1}{g_m}$

$R_{OUT} = R_D$	(zero V_{IN})

Common Drain Amp

T-model, no r_o (ignore)



$$R_{IN} = \infty$$

For R_{out}, zero V_{in}

$$R_{OUT} = 1/g_m$$

$$V_{out} = iR_L = \frac{V_{in}}{\frac{1}{g_m} + R_L} \times R_L$$

$$\frac{V_{out}}{V_{in}} = \frac{R_L}{\frac{1}{g_m} + R_L} \quad \text{(voltage division)}$$

$$\text{Gain} = \frac{R_L}{1/g_m + R_L}$$

Basic MOSFET Amplifier Characteristic Summary

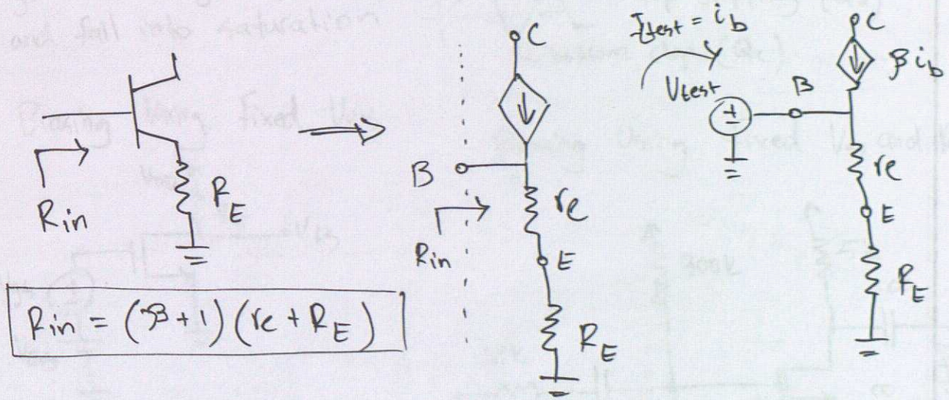
	Rin	Gain	Rout
Common Source	∞	$-g_m R_D$	R_D
Common Source w/h R_S	∞	$-\frac{g_m R_D}{1+g_m R_S}$	R_D
Common Gate	$\frac{1}{g_m}$	$g_m R_D$	R_D
Source Follower (Common Drain)	∞	1	$\frac{1}{g_m}$

BJT Versions

- common source (MOSFET) → common emitter (BJT)
- common gate (MOSFET) → common base (BJT)
- common drain (MOSFET) → common collector (BJT)

Resistance Reflection Rule for BJT's

the resistance looking into the base is $(\beta+1)$ times the total resistance in the emitter (including ~~R_E~~) r_e



$$R_{in} = (\beta+1)(r_e + R_E)$$

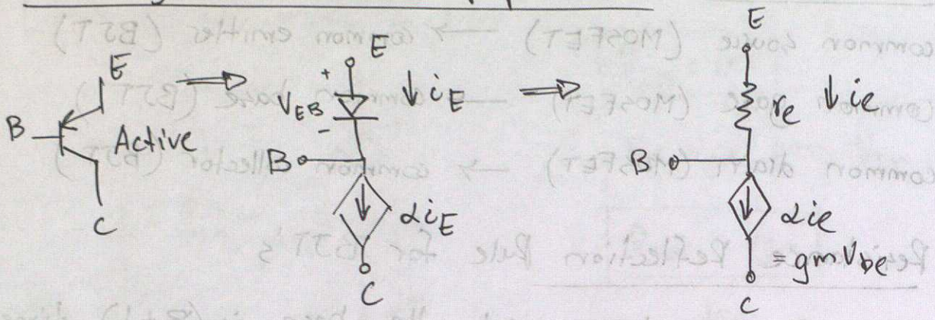
Common Emitter: $R_{in} = (\beta+1) r_e = r_\pi$

Common Emitter with R_E: $R_{in} = (\beta+1)(r_e + R_E)$ ← added to increase Rin

Common Base: $R_{in} = r_e = \alpha/g_m$

Emitter Followers: $R_{in} = (\beta+1)(r_c + R_c)$

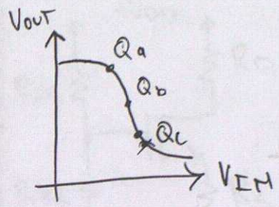
Small Signal Model for pnp BJT

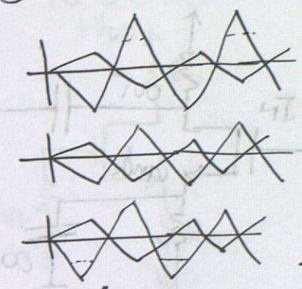


- basically the same as npn case, except it's V_{EB}, not V_{BE}

Biasing

- establishing an operating point Q



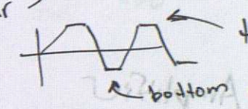


slope lower at Q_a, but risk of clipping @ top

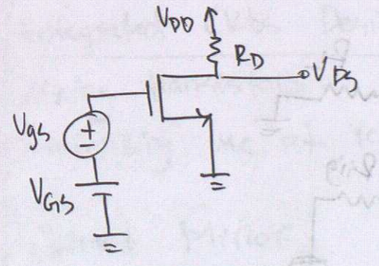
slope at Q_b is (-)ve, so we invert and have a gain

slope steeper at Q_c, so we have higher gain

you might "clip" your Vout if you go too far and fall into saturation

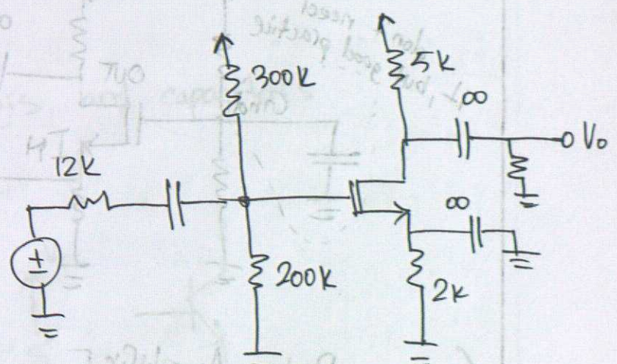


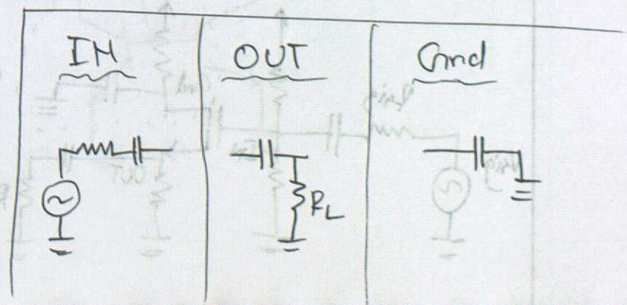
Biasing Using fixed V_{GS}



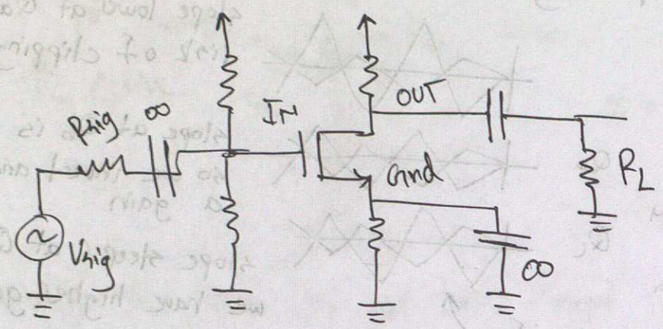
* must have voltage src
* drain current drops by 75%.

Biasing Using fixed V_{GS} and R_S

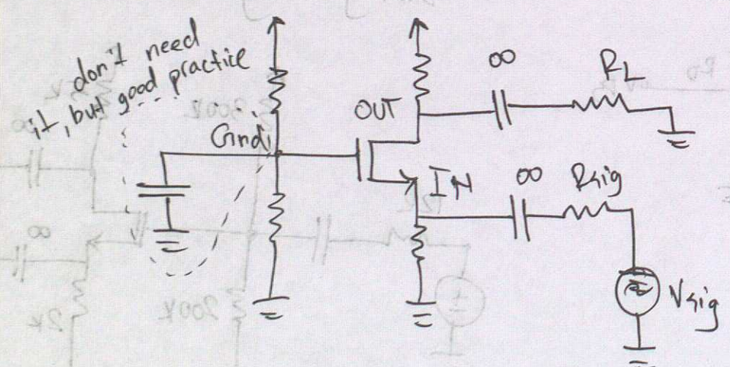




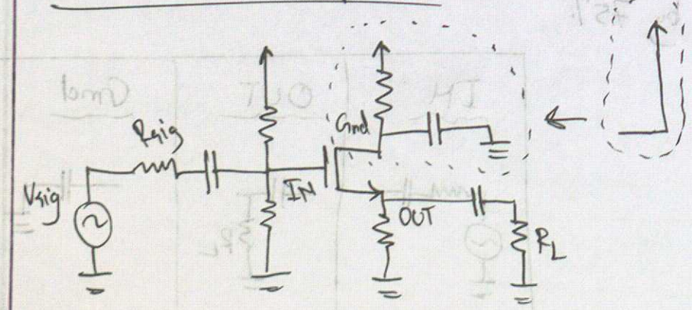
Common Source Amplifier



Common Gate Amplifier

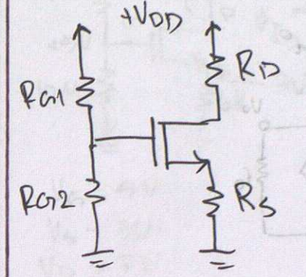


Common Drain Amplifier

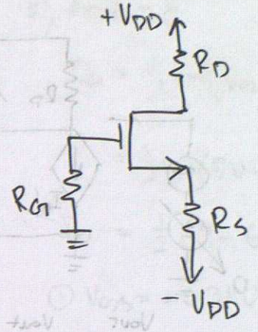


Common Bias Ckts

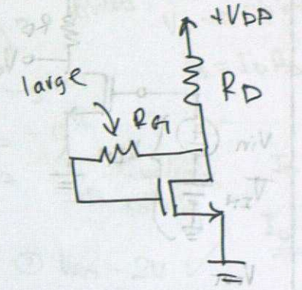
Single Supply



Two Supplies



Using drain-gate feedback resistor



Discrete Ckts Design

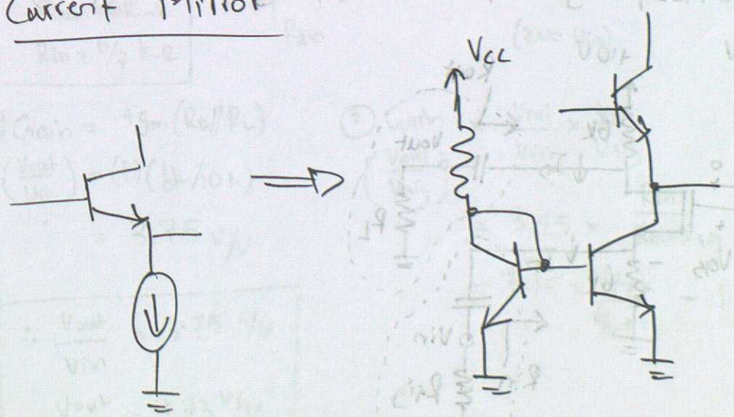
→ Varying discrete components (resistor, capacitor etc...)

Integrated Ckts Design

→ sizing transistors

→ minimizing use of resistors and capacitors

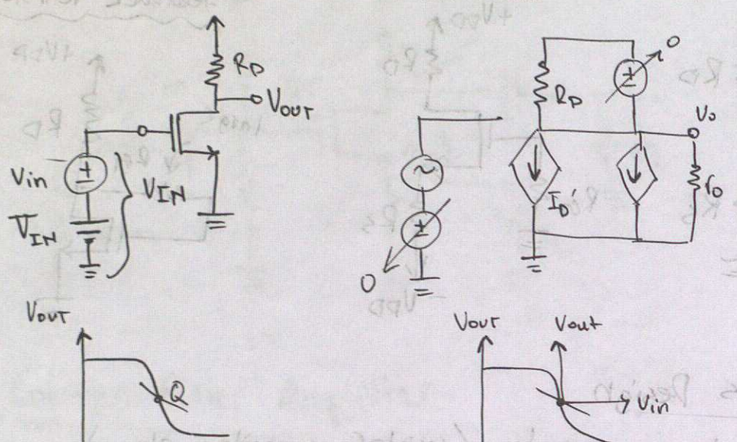
Current Mirror



Week 10: Lecture 3 — Nov 15, 2024

Analyzing Transistor Amplifiers

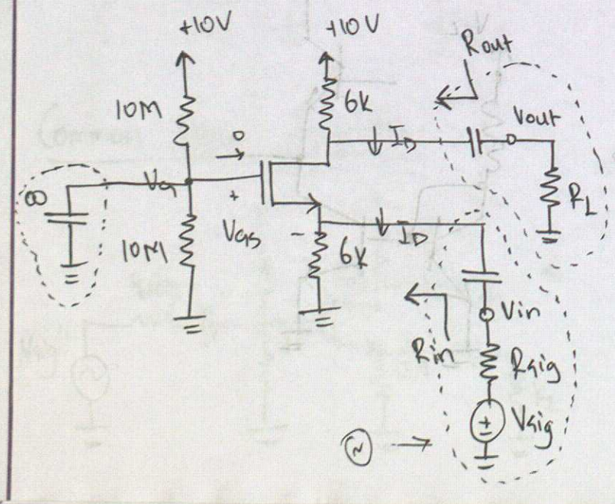
Nonlinear — Linearize



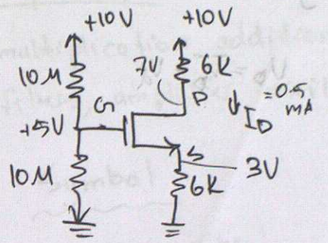
Ex 1: MOSFET Amplifier: Determine Gain, R_{out}, R_{in}

$\mu_n C_{ox}\left(\frac{W}{L}\right) = 1\ \frac{mA}{V^2}$, $V_t = 1V$, $\lambda = 0$, $V_{DD} = 10V$, $R_D = R_S = 6k\Omega$,

$R_{G1} = R_{G2} = 10M\Omega$, $R_{sig} = 1k$, $R_L = 10k$, V_{sig} is 100mV (peak) sine wave



Step 1: Find operating point Q (DC Analysis) [V, mA, kΩ]



$V_G = 5V$
$V_S = 3V$
$V_D = 7V$

1) Assume SATURATION

2) Analyze — voltage divides, $V_G = 5V$; $V_S \Rightarrow$ Ohm's Law, $V_S = I_D R_S$

$I_D = \frac{1}{2} k_n (V_{GS} - V_t)^2$ ← given

$= \frac{1}{2}(1)(5V - I_D R_S - 1)^2$

$I_D = \frac{1}{2}(4 - 6I_D)^2 \Rightarrow$ Quadratic solving

① $I_D = 0.89\ mA$ ② or $I_D = 0.5mA$

① $V_{GS} = -0.34V$ ✗ ② $V_{GS} = 2V$ ✓

Step 2: Derive and Analyze small-signal ckt

$r_o = \frac{1}{\lambda I_D} \Rightarrow \infty$ since $\lambda = 0$

$g_m = \frac{2I_D}{V_{OV}} = \frac{2(0.5mA)}{2-1V} = 1\ \frac{mA}{V}$

$\frac{1}{g_m} = \frac{1V}{1mA} = 1k\Omega$

$\therefore R_{out} = 6k\Omega$
$R_{in} = 6/7\ k\Omega$

$R_{out} = R_D$ (zero V_{in})

$R_{IN} = \frac{1}{g_m} \| R_S$
$= 1k \| 6k$
$= 6/7\ k\Omega$

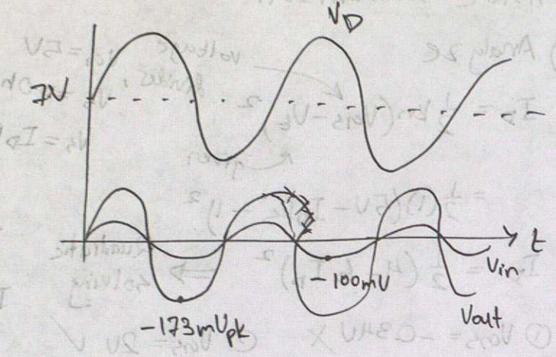
① Gain $\left(\frac{V_{out}}{V_{in}}\right) = +g_m(R_D \| R_L)$
$= (1)(6k/10k)$
$= 3.75\ V/V$

② Gain $\left(\frac{V_{out}}{V_{sig}}\right) = \frac{V_{out}}{V_{in}} \times \frac{V_{in}}{V_{sig}}$
$= 3.75 \times \frac{R_{in}}{R_{in} + R_{sig}}$
$= 3.75 \times \frac{6/7k}{6/7k + 1} = 1.73\ V/V$

$\therefore \frac{V_{out}}{V_{in}} = 3.75\ V/V$

$\frac{V_{out}}{V_{sig}} = 1.73\ V/V$

Step 3: Recombine to create total signal

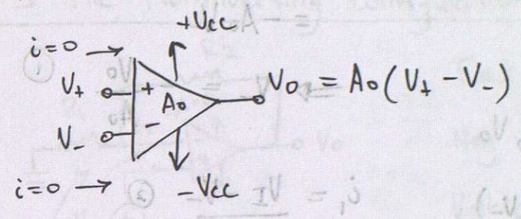


$V_D = \bar{V}_D + v_d$

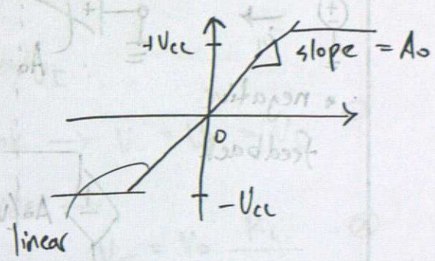
Op Amps

- multiplication, addition, subtraction, integration, differentiation
- filters, amplifier, oscillators

Symbol



Transfer Characteristic

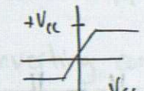


Properties of Op Amps (ideal)

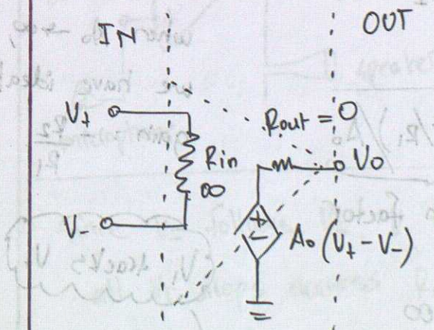
$i_+ = i_- = 0$

gain $A_o \to \infty$

*strange device on its own. you have to add feedback



Model

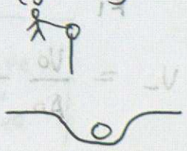


∴ Stick:

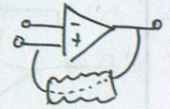
Use Feedback to Use Op Amps

Negative:

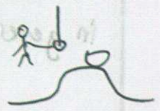
output is fed to (-)ve terminal (generally stable)



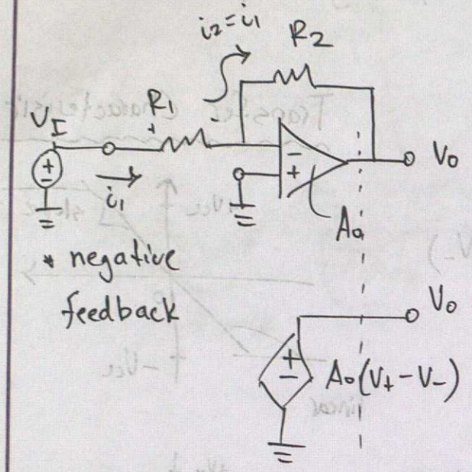
Positive:



output is fed to (+)ve terminal (generally unstable)



2.2 Inverting Amplifier (ideal)



* negative feedback

Find Gain: $G = \frac{V_o}{V_I}$

$V_o = A_o(V_+^{\,0} - V_-)$

$= -A_o V_-$

$\Rightarrow V_- = -\frac{V_o}{A_o}$ ①

$i_1 = \frac{V_I - V_-}{R_1}$ ②

$i_2 = i_1$

KVL: $V_o = V_- - (i_2)(R_2)$ ③

now sub ①, ② → ③

$V_o = -\frac{V_o}{A_o} - \left(\frac{V_I - (-V_o/A_o)}{R_1}\right)(R_2)$

$V_o\left(1 + \frac{1}{A_o} + \frac{R_2}{R_1}\frac{1}{A_o}\right) = -\frac{R_2}{R_1} V_I$

$\frac{V_o}{V_I} = \underbrace{-\left(\frac{R_2}{R_1}\right)}_{\text{ideal gain}} \times \underbrace{\frac{1}{1 + (1 + R_2/R_1)/A_o}}_{\text{correction factor}}$

when $A_o \to \infty$, we have ideal gain : $-\frac{R_2}{R_1}$

$= -\frac{R_2}{R_1}$ for $A_o \to \infty$

V_1 tracks V_+

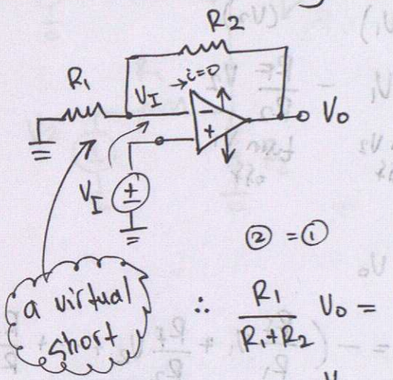
in general: $V_+ - V_- = \frac{V_o}{A_o} \to 0 \Rightarrow \therefore V_- \simeq V_+$

Quick Analysis of Ideal Op Amp

Assume 1) $\boxed{i_+ = i_- = 0}$ → device characteristic

2) $\boxed{V_- = V_+}$ → negative feedback characteristic

2.3 The Noninverting Configuration



Find V_o/V_I:

Neg fdbk → $V_- = V_+ = V_I$ ①

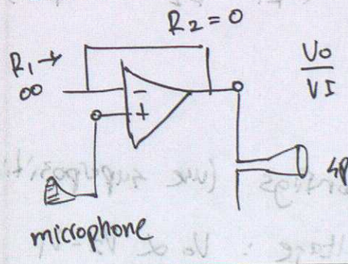
Volt divider → $V_- = V_o \frac{R_1}{R_1 + R_2}$ ②

② = ①

$\therefore \frac{R_1}{R_1 + R_2} V_o = V_I$

$\frac{V_o}{V_I} = \frac{R_1 + R_2}{R_1} \Rightarrow$ noninverting config. $\boxed{\frac{V_o}{V_I} = 1 + \frac{R_2}{R_1}}$

Extreme:

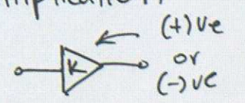


$\frac{V_o}{V_I} = 1 + \frac{R_2}{R_1} = 1$

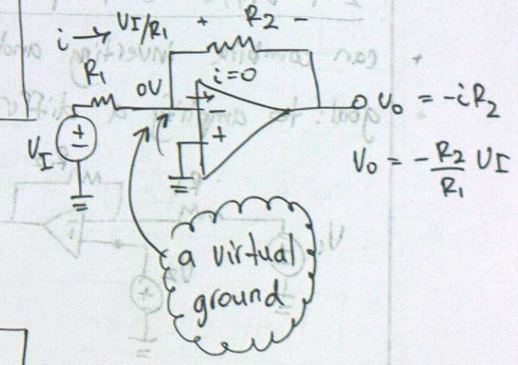
Since V_- follows V_+, $V_- = 0V$

$\therefore$ all V_I drops accross R_1, $i = \frac{V_I}{R_1}$

Math operation : multiplication by a scalar k :

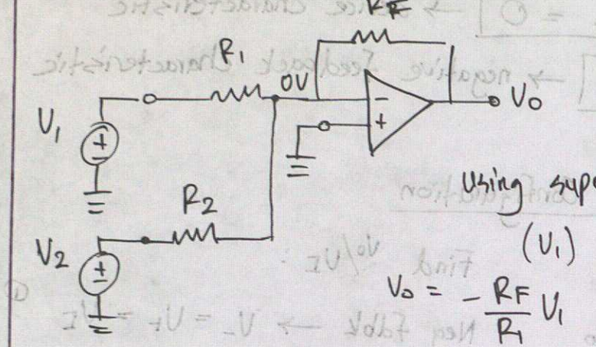


2.2 Inverting Config (quick analysis)



Addition

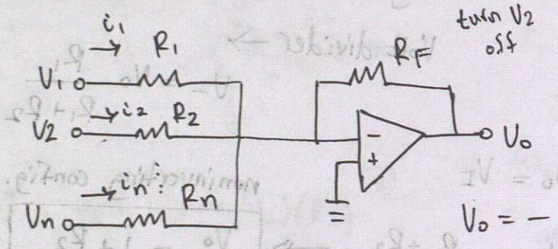
R_F feedback resistor



- exploit the virtual ground at V−
- application: audio mixer

Using superposition:

$$V_o = \underbrace{-\frac{R_F}{R_1} V_1}_{\text{turn } V_2 \text{ off}} \underbrace{-\frac{R_F}{R_2} V_2}_{\text{turn } V_1 \text{ off}}$$



$$V_o = -\left(\frac{R_f}{R_1} V_1 + \frac{R_f}{R_2} V_2 + \cdots + \frac{R_f}{R_n} V_n\right)$$

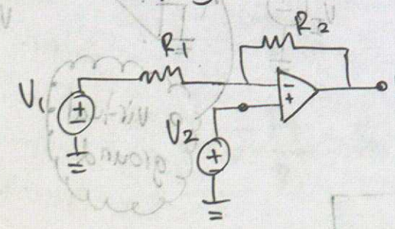
$$= -R_F\left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \cdots + \frac{V_n}{R_n}\right)$$

Math Operation: weighted sum amplifier

2.4 Difference Amplifier

- can combine inverting and noninverting configs (use superposition)

goal: to amplify a differential input voltage : $V_o \propto V_2 - V_1$

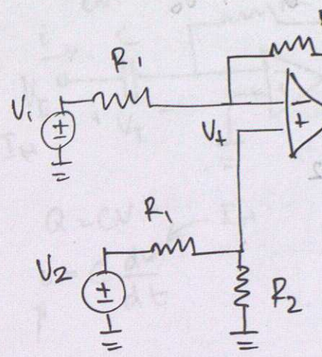


$$V_o = \underbrace{\left(1 + \frac{R_2}{R_1}\right) V_2}_{\text{turn } V_1 \text{ off}} + \underbrace{\left(-\frac{R_2}{R_1}\right) V_1}_{\text{turn } V_2 \text{ off}}$$

$$= K(V_2 - V_1)$$

$$V_o = \underbrace{\left(1 + \frac{R_2}{R_1}\right)}_{K+1} V_2 - \underbrace{\frac{R_2}{R_1}}_{K} V_1$$

we attenuate V_2 slightly by adding a voltage divider



$$V_o = \left(1 + \frac{R_2}{R_1}\right) V_+ - \frac{R_2}{R_1} V_1$$

$$= \left(\frac{R_1 + R_2}{R_1}\right)\left(\frac{R_2}{R_1 + R_2} V_2\right) - \frac{R_2}{R_1} V_1$$

$$= \frac{R_2}{R_1} V_2 - \frac{R_2}{R_1} V_1$$

$$\therefore V_o = \frac{R_2}{R_1}(V_2 - V_1)$$

Math operation: subtraction

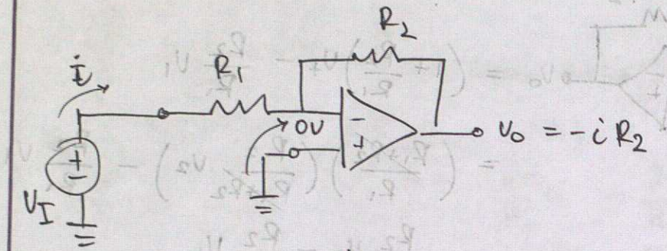
2.5.2 Integration

recall inverting config

$\times -R_2$

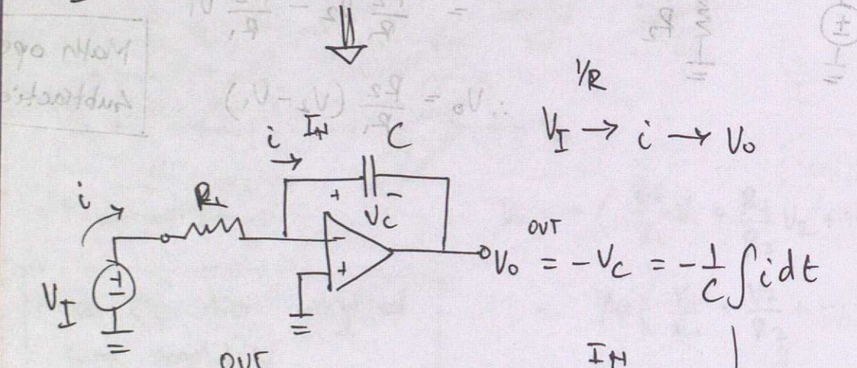
$1/R_1 \quad -\times R_2 = -\frac{R_2}{R_1}$

$V_I \rightarrow i \rightarrow V_o$

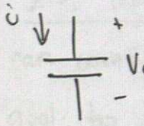


$\Downarrow$ $1/R$

$V_I \rightarrow i \rightarrow V_o$



$Q = CV \rightarrow V_c = \frac{Q}{C} = \frac{1}{C}q = \frac{1}{C}\int i\,dt$



$V_o = -\frac{1}{C}\int \frac{V_I}{R} dt$

$\therefore V_o = -\frac{1}{RC}\int V_I\, dt$ ← inverting integrator

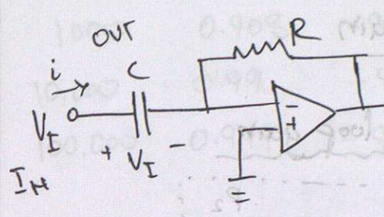
Math Operation: Integrator

2.5.3 Differentiation

$\frac{d}{dt} \times -R$

$V_I \rightarrow i \rightarrow V_o$

swap R and C



Math operation: differentation

$Q = CV$ ← I_H

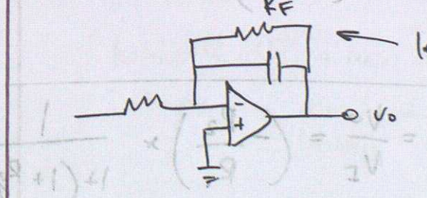
$i = C\frac{dV}{dt}$

OUT

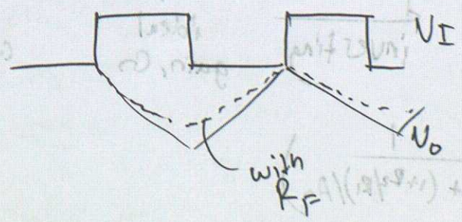
$\therefore V_o = -RC\frac{d}{dt}V_I$ inverting differentiator

Notes

- integrators are less noisy
- differentiators can be noisy, instability issues
- in practice, add a resistor in parallel to capacitor for feedback at DC



← lets path exist in DC for feedback (very large: eg. 1MΩ)



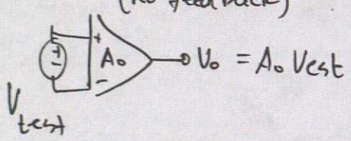
Op Amp nonidealities

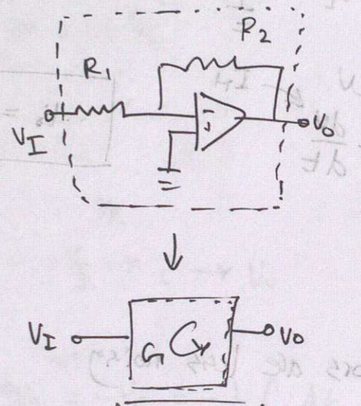
2.6 : Effect of finite op amp gain

Open-loop gain V_S **closed loop gain**

A_0 opamp gain (Device)

(no feedback)

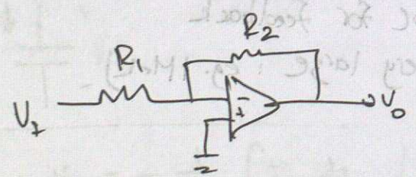




$$G = \frac{V_0}{V_I} \left(= -\frac{R_2}{R_1}\right)$$

(circuit)

2.2.2 Effect finite op amp on inverting config



$$G = \frac{V_0}{V_I} = \left(-\frac{R_2}{R_1}\right) \times \frac{1}{1+(1+R_2/R_1)/A_0}$$

inverting — ideal gain, G_1 — correction factor

Non-inverting

$$G = \frac{V_0}{V_I} = \left(1+\frac{R_2}{R_1}\right) \times \frac{1}{1+(1+R_2/R_1)/A_0}$$

↑ only difference

ex: $R_2 = 100\,k\Omega$, $R_1 = 1k\Omega$ $\rightarrow G_1 = -\frac{100}{1} = -100\,V/V$

A_0	correction	G_1	error
1000	0.908	-90.8	-9% error
10,000	0.99	-99	-1% error ← big enough
100,000	0.999	-99.9	-0.1% error

good enough if $A >> 1 + \frac{R_2}{R_1}$

2.8: Large Signal Limitations

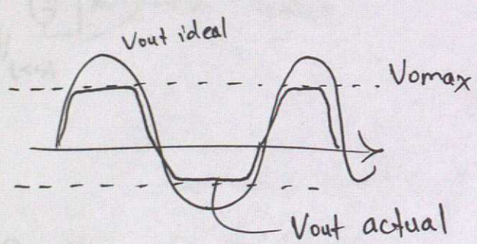
741: $A_0 \approx 100.000$ V/V

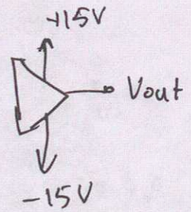
2.8.1: output voltage saturation, $V_{omax} = \pm 12.14V$
(maximum voltage output)

2.8.2: output current saturation, $I_{omax} = \pm 25mA$

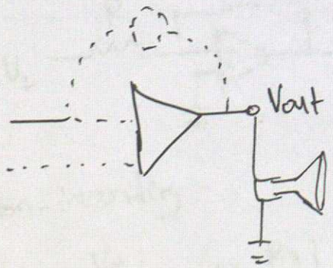
2.8.3: slew rate, $SR = \pm 0.5$ V/μs

2.8.1: depends on power supply (e.g. ±15V, ±12V)





2.8.2: I_{omax} (e.g. 25mA), we can't attach a load that draws too much current

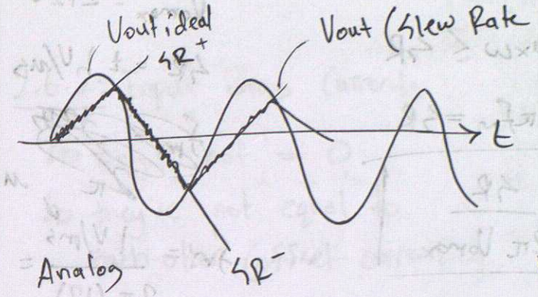


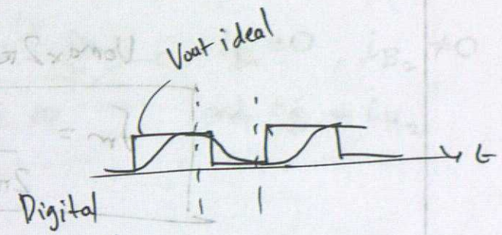
$V_{out\,max} = I_{omax} \times R_L$
$= 25mA\,(10\Omega)$
$= 0.25V$

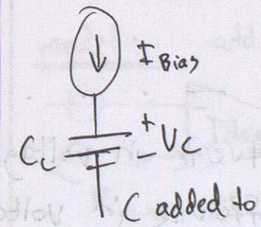
not enough because not enough current

2.8.3: Slew Rate

- the maximum rate of change of the output voltage [V/seconds]







$Q = CV$

$i = C_L \frac{dV_C}{dt}$

$\frac{dV_C}{dt} = \frac{i}{C_2}$ ← I_{Bias} (fixed), ← C_2 fixed

} this is how we fix the slew rate

Full power Bandwidth (f_M)

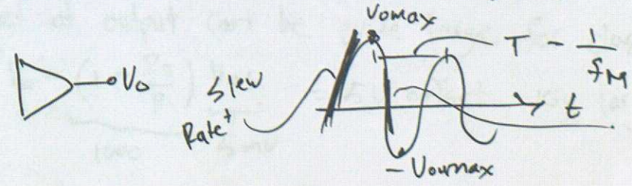
f_M represents the max frequency sine wave at the max output voltage (peak) without slew rate distortion

$V_o(t) = V_{omax} \cos \omega t$

$\frac{dV_o(t)}{dt} = V_{omax} \omega \times (-\sin \omega t)$

$V_o(t) = V_{omax} \times (2\pi f(t))$

$\frac{dV_o(t)}{dt} =$



$V_{out}(t) = V_{omax}\cos(\omega t)$

$\frac{d}{dt} V_{out}(t) = V_{omax}\,\omega(-\sin(\omega t))$

set $V_{omax}\omega \le SR$

$V_{omax} 2\pi f_M = SR$

$$f_m = \frac{SR}{2\pi V_{omax}}$$

e.g. for 741

$V_{omax} = \pm 12\,V$

$SR = \pm 1\,V/\mu s$

$f_m = \frac{1\,V/\mu s}{2\pi(12)} = 13\,kHz$

V_{out} (pk)	max freq
12V	13 kHz
÷10 ↓ 1.2V	130kHz ↓ ×20

- negative feedback: V_o tries to reduce difference in voltage
- positive feedback: V_o tries to increase difference in voltage

Sec. 2.6: DC Imperfections

2.6.1: Offset Voltage: $V_o \neq 0$ in practice (transistors can have diff. β's)

2.6.2: Input Bias Currents: $i \neq 0$

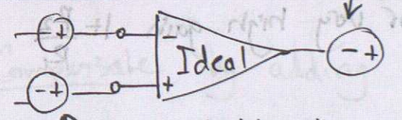
- they're not $= 0$
- they're not equal to each other (offset current)

$i_{B_1} \neq 0$, $i_{B_2} \neq 0$ and $i_{B_1} \neq i_{B_2}$

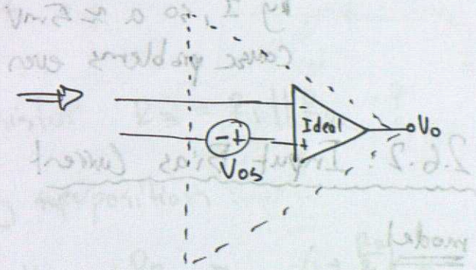
Main Idea: Model → Analyze → Avoid or Compensate

→ **2.6.1 – Offset Voltage**

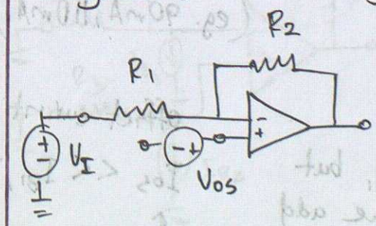
model: add a voltage source



we will take this one



analyze (inverting config)



using superposition

$$V_o = \left(1 + \frac{R_2}{R_1}\right) V_{os} \quad \text{(due to } V_{os}\text{)}$$

non-inverting config has V_I attached to V_+ terminal (in series w/ V_{os})

Offset at output can be quite large for closed loop gains

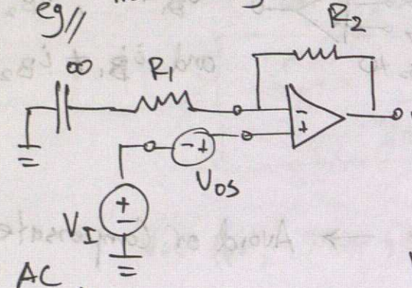
e.g. $V_o = \underbrace{\left(1 + \frac{R_2}{R_1}\right)}_{1000} \underbrace{V_{os}}_{5\,mV} = 5\,V$ offset, very large!

Compensating

1) Trimming with potentiometer

2) for AC signals, can add AC coupling capacitor

eg// non-inverting:



using superposition

Input ← due to → offset

$$V_o = \left(1+\frac{R_2}{R_1}\right)V_I + \left(1+\frac{R_2}{R_1+\infty}\right)V_{OS}$$

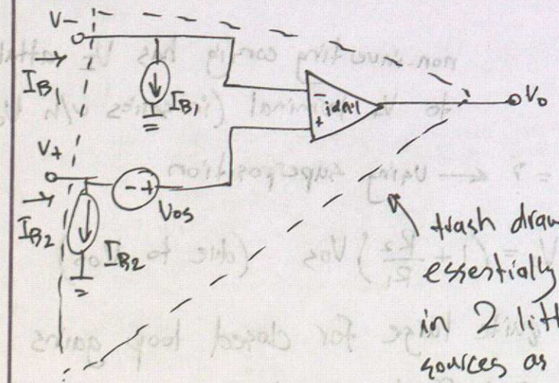
↑ capacitor

$$V_o = \left(1+\frac{R_2}{R_1}\right)V_I + (1)V_{OS}$$

* this capacitor essentially makes V_{OS} multiplied by 1, so a ≈ 5mV offset is fine and won't cause problems even for very high gain $1+\frac{R_2}{R_1}$

2.6.2: Input Bias Current

model



trash drawing, but essentially we add in 2 little current sources as a model inside

input bias currents:

I_{B1}, I_{B2}

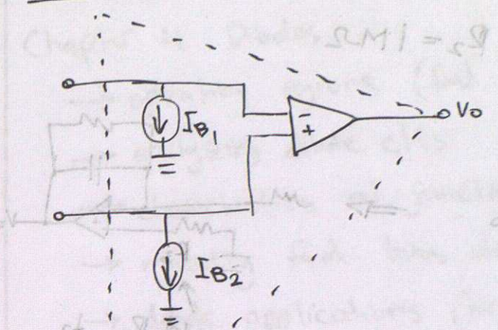
(eg. 90mA, 110mA)

offset current:

$I_{OS} << I_{B1}, I_{B2}$

↑ offset is much less than the actual currents

MODEL:



ANALYZE

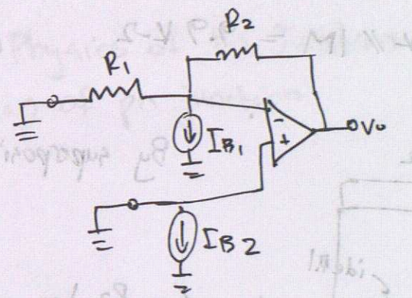
(same for inverting and non-inverting)

using superposition:

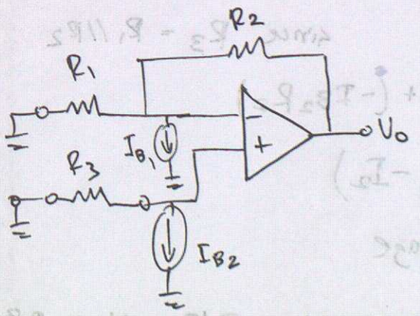
$$V_o = +\underline{R_2} I_{B1} + \underline{\emptyset} I_{B2}$$

$V_o = R_2 I_{B1}$ ← output only depends on I_{B1} (I_{B2} does not have any effect)

if R_2 larger, we would get big voltage error.



Compensate by adding Resistor $R_3 = R_1 \| R_2$



By superposition:

$$V_o = +R_2 I_{B1} + \left(1+\frac{R_2}{R_1}\right)(-I_{B2}R_3)$$

V_+

$$V_o = R_2 I_{B1} + \left(1+R_2/R_1\right)(-I_{B2}R_3)$$

$$= R_2 I_{B1} - \left(\frac{R_1+R_2}{R_1}\right)\left(\frac{R_1 R_2}{R_1+R_2}\right) I_{B2}$$

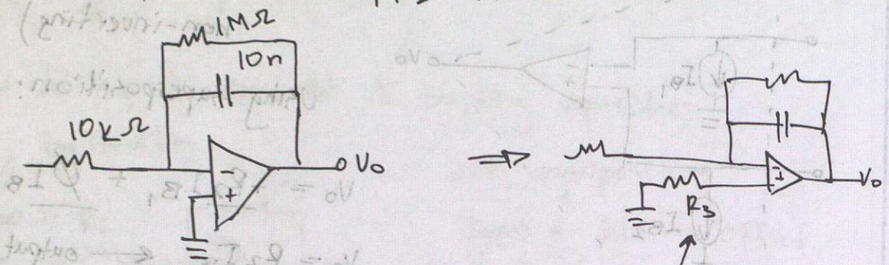
$$= R_2\underbrace{(I_{B1}-I_{B2})}_{I_{OS}} = \begin{cases} 0 & \text{if } I_{B1}=I_{B2} \\ \pm R_2 I_{OS} \end{cases}$$

I_{OS} offset

Week 13 : Lecture 1 — Dec 3, 2024

Ex: Miller Integrator $R_1 = 10K$, $C = 10nF$, $V_{os} = 3mV$

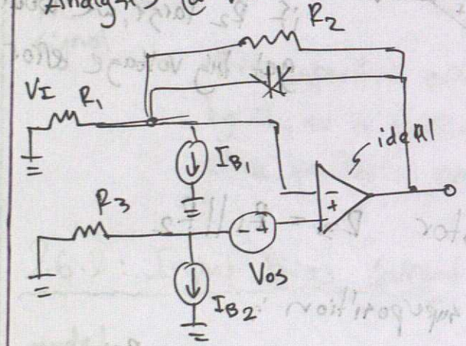
$I_B = 100nA$, $I_{os} = 10nA$, $R_2 = 1M\Omega$



add R_3 to deal with input bias current

a) $R_3 = R_1 // R_2 = 10K // 1M = 9.9K\Omega$

Analysis @ DC



By superposition :

$$V_o = \left(1 + \frac{R_2}{R_1}\right) V_{os} + I_{B_1} R_2 + \underbrace{\left(1 + \frac{R_2}{R_1}\right)(-I_{B_2} R_3)}$$

since $R_3 = R_1 // R_2$

$$\Rightarrow V_o = \left(1 + \frac{R_2}{R_1}\right) V_{os} + I_{B_1} R_2 + (-I_{B_2} R_2)$$

$$= \left(1 + \frac{R_2}{R_1}\right) V_{os} + R_2 (I_{B_1} - I_2)$$

worst case positive dc output voltage

$$V_o = \left(1 + \frac{1000k}{10k}\right)(+3mV) + (1000k)(10mA) = 313\ mV \approx 0.3V$$

↳ $+313mV$ would be max negative

Course Review

- Chapter 4 Diodes
  - → operating regions (fwd bias, rev bias, breakdown)
  - → analyzing diode ckts
  - → characteristics of junction diodes
  - → modeling fwd bias diode (ideal, CVD,
  - → diode applications (rectifiers, limiting, clamping ckts)
- Chapter 3 Physics of Pn Junction
  - → operation of pn junction